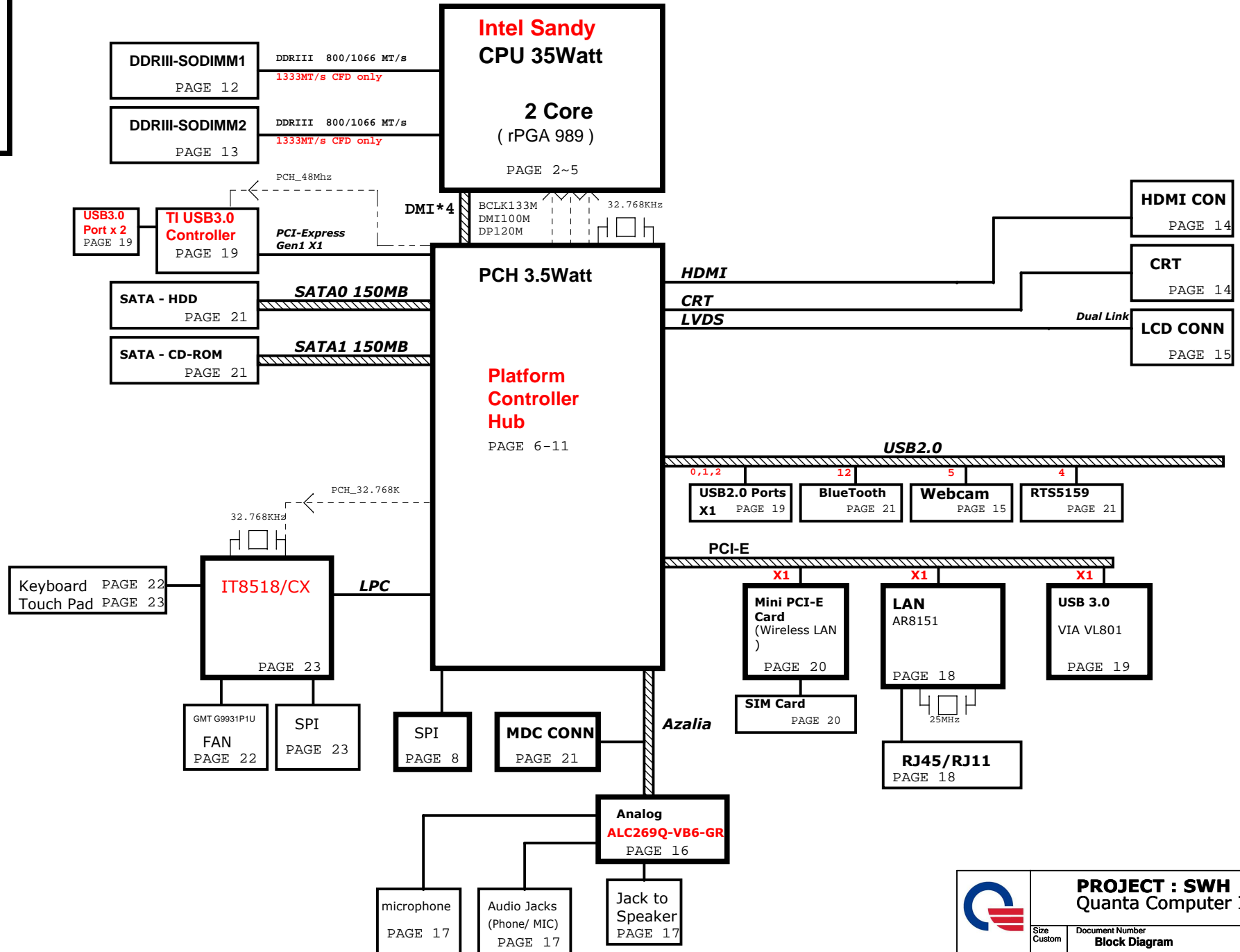
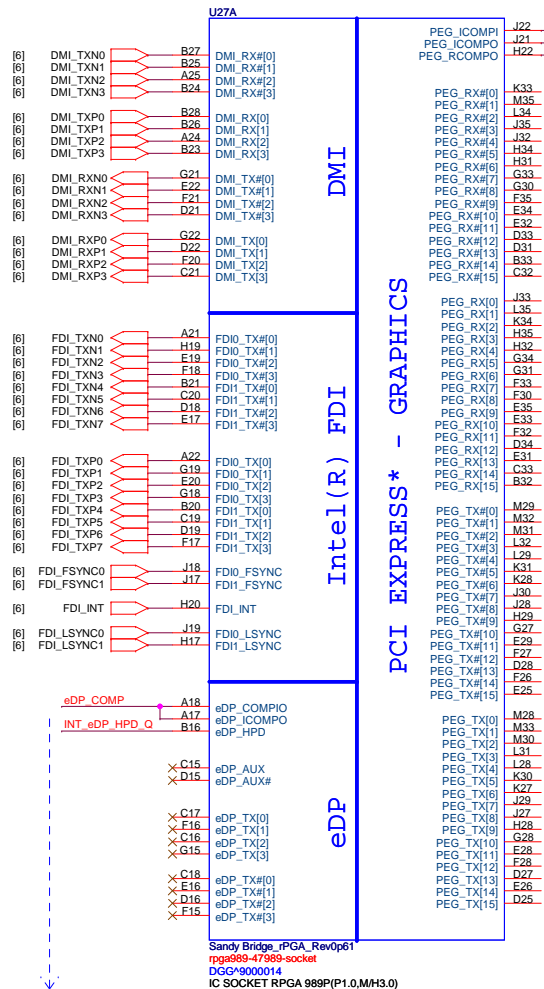


SWH_UMA (14") BLOCK DIAGRAM

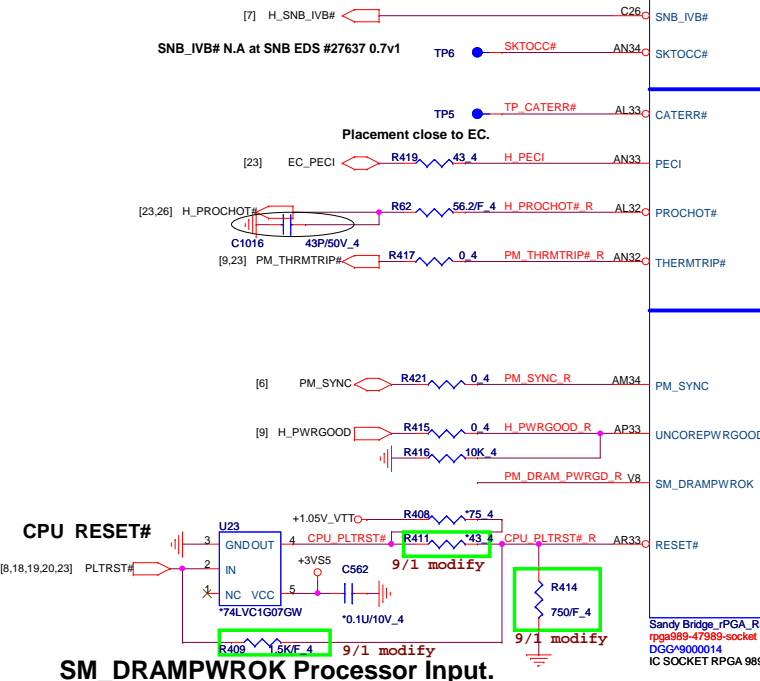
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(high)
LAYER 4 : IN2(low)
LAYER 5 : VCC
LAYER 6 : BOT



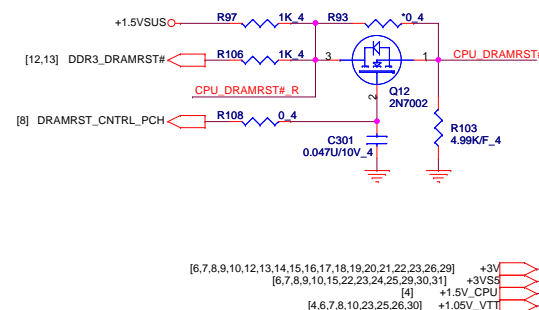
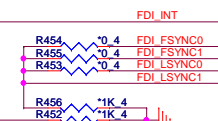


eDP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.

PEG_COMP connect to PIN H22/J22 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN J21 W:12mils/S:15mils/L: 500mils.



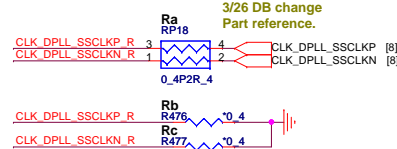
DDR3 DRAM RESET

FDI disable
(DIS only stuff)

FDI_FSYNCK can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

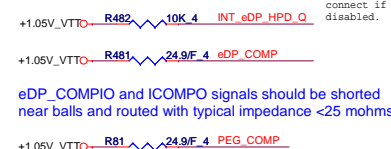
PEG x16 disable (UMA only remove)

Embedded Display PLL Clock



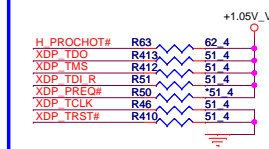
	Ra	Rb	Rc
DiS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

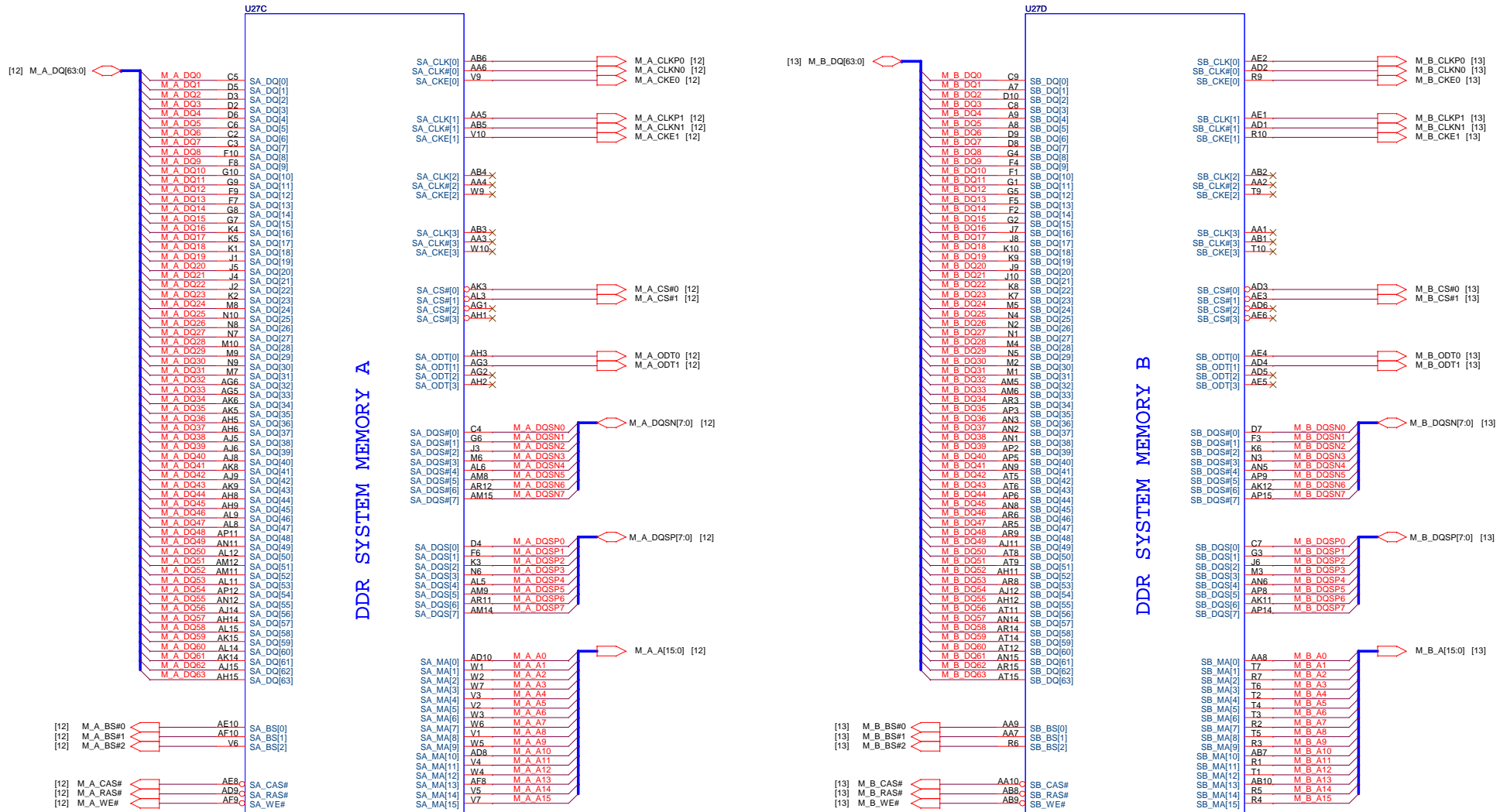
Processor pull-up (CPU)

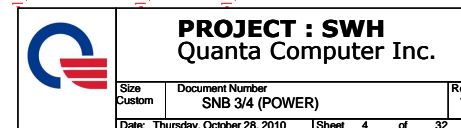
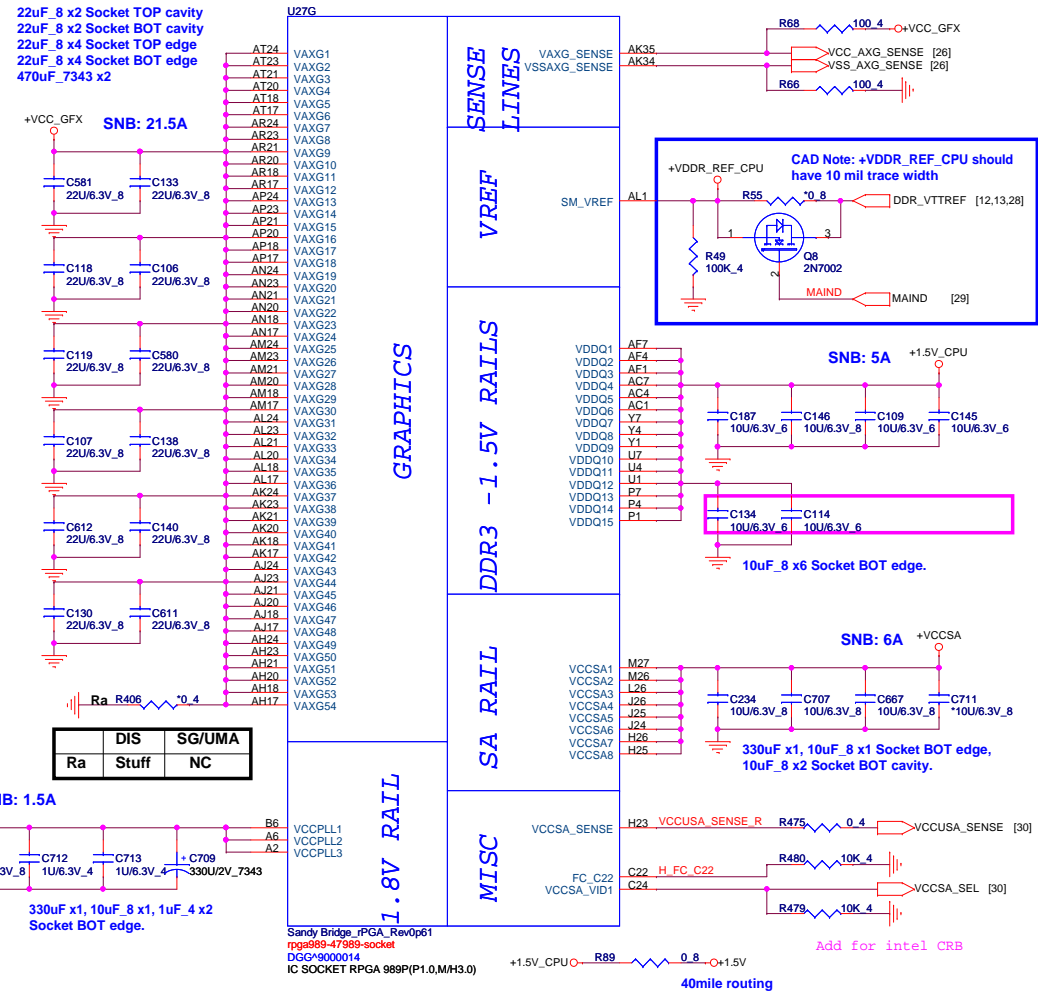


PROJECT : SWH
Quanta Computer Inc.

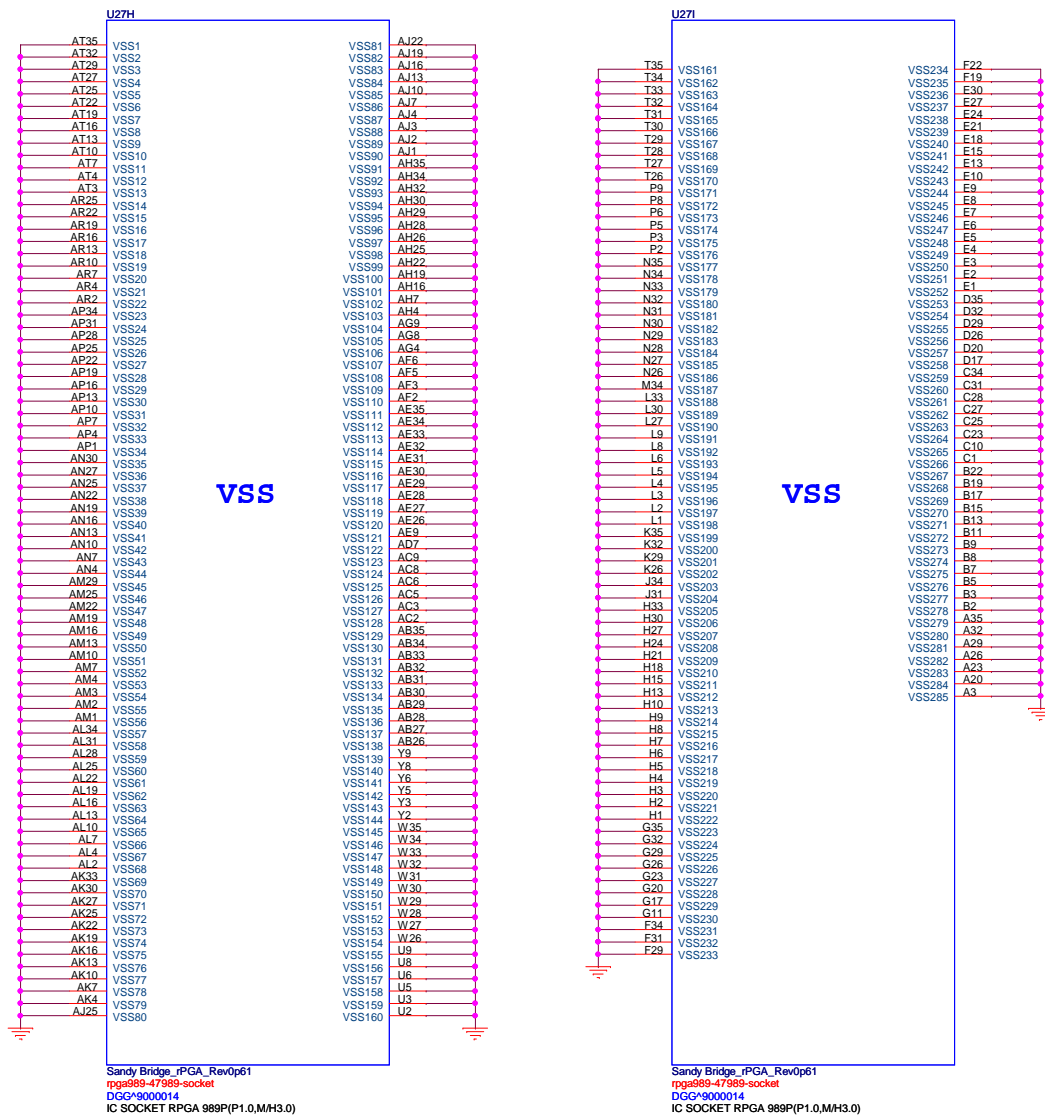
Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A
Date: Thursday, October 28, 2010	Sheet 2 of 32	

Sandy Bridge Processor (DDR3)





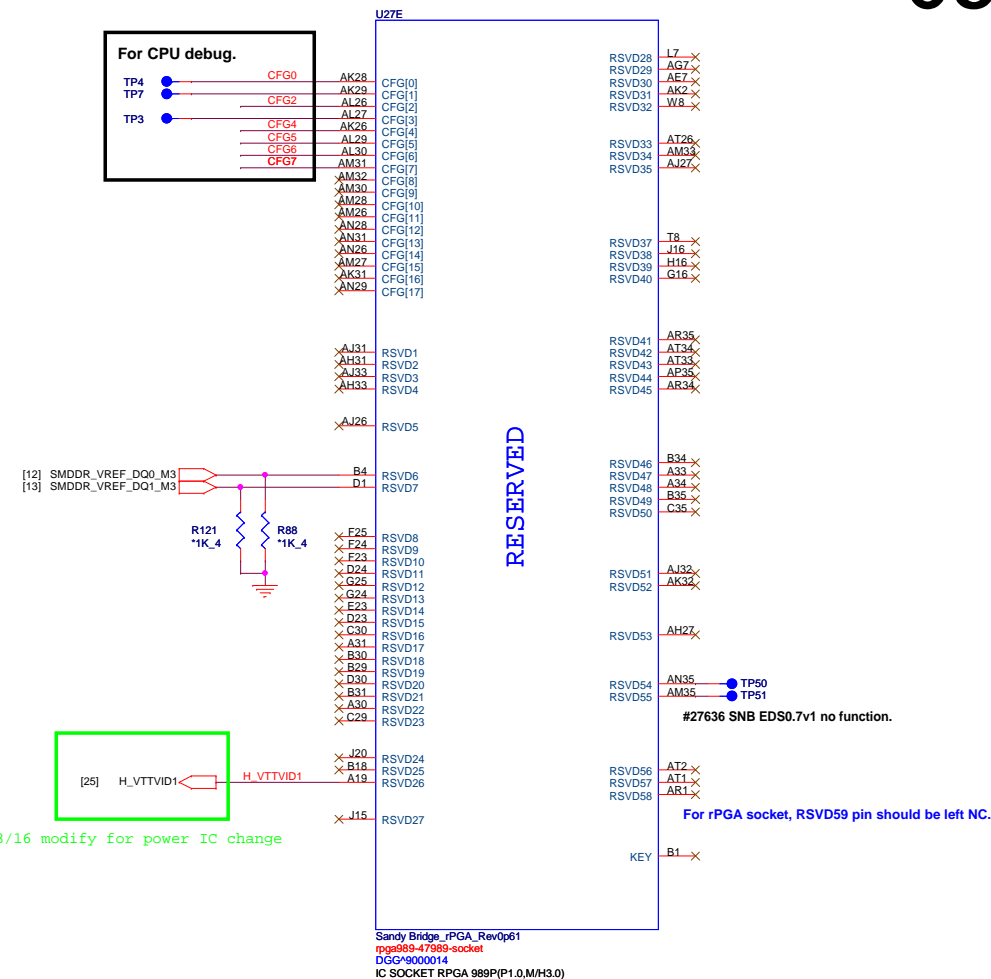
Sandy Bridge Processor (GND)



Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

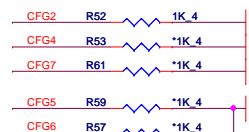
Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

Sandy Bridge Processor (RESERVED, CFG)



CFG[6:5] (PCIe Port Bifurcation Straps)

```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

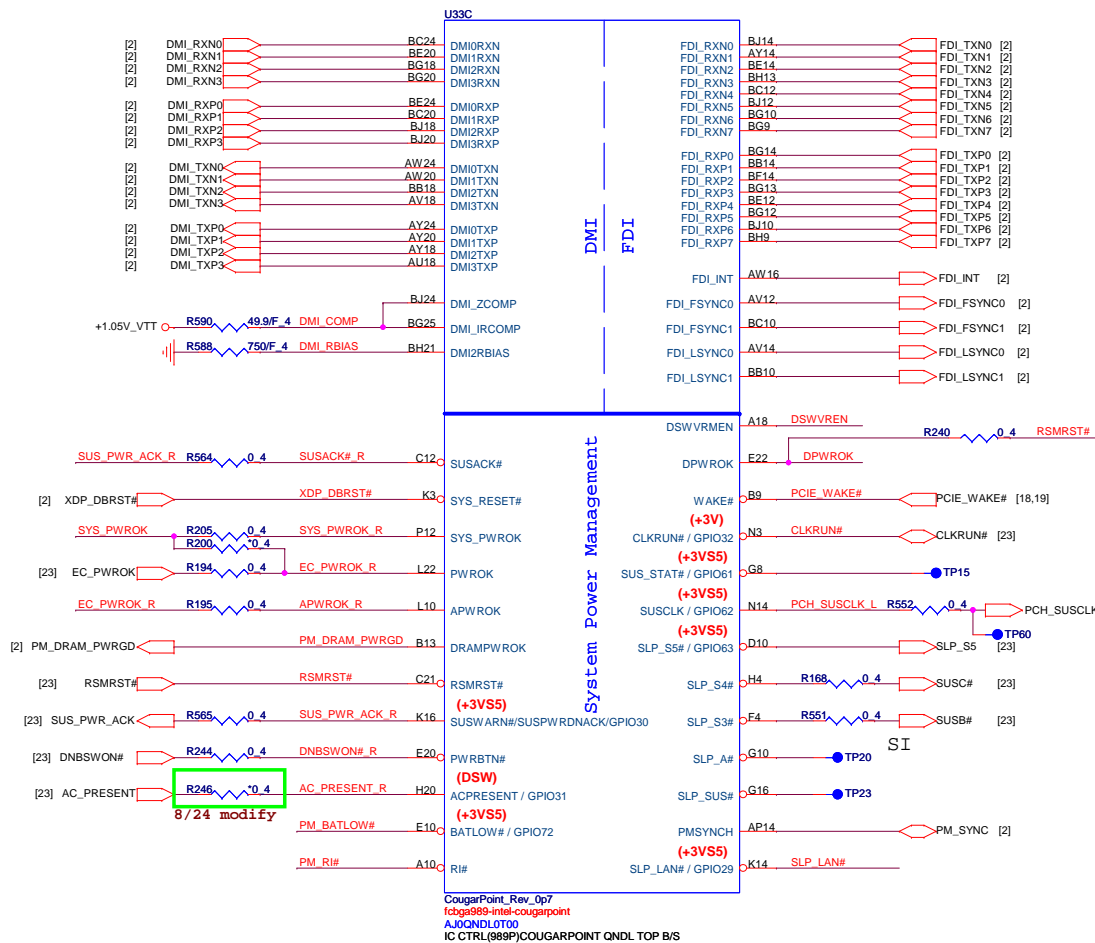
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



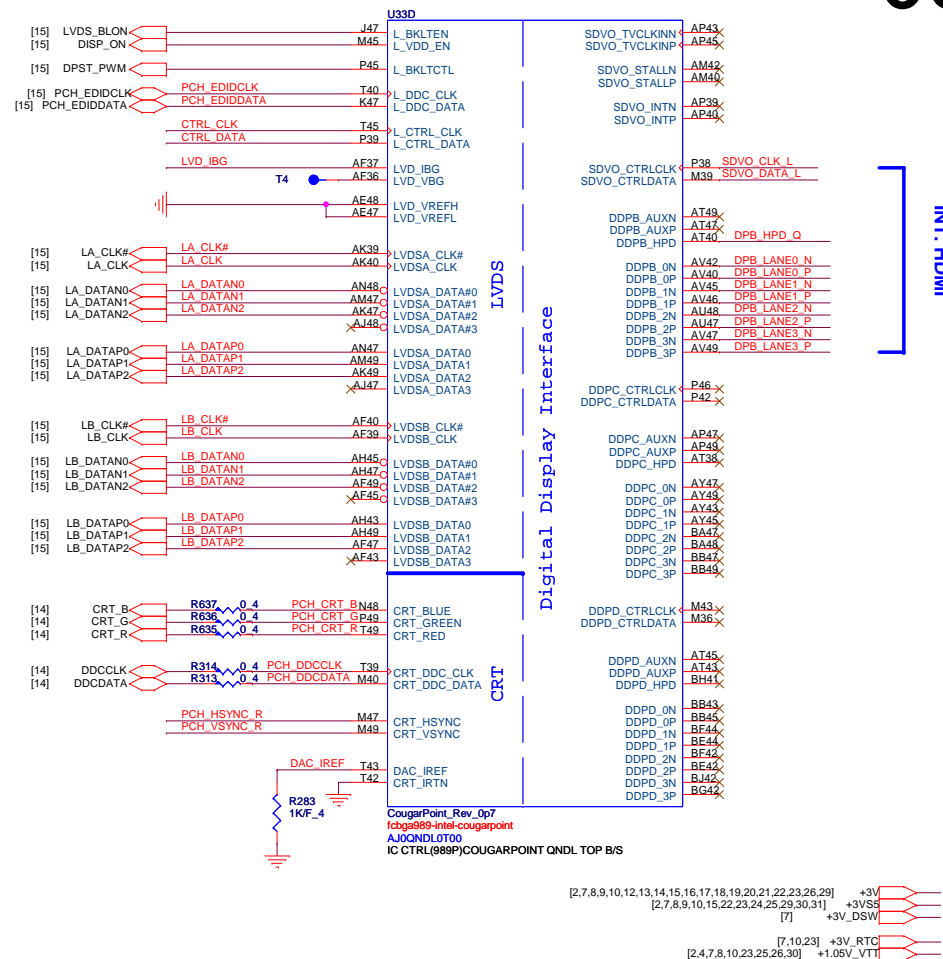
PROJECT : SWH
Quanta Computer Inc.

Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
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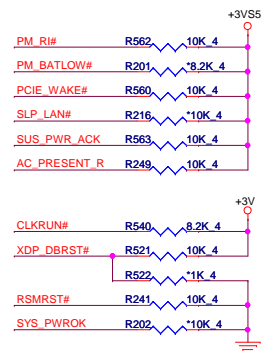
Cougar Point (DMI,FDI,PM)



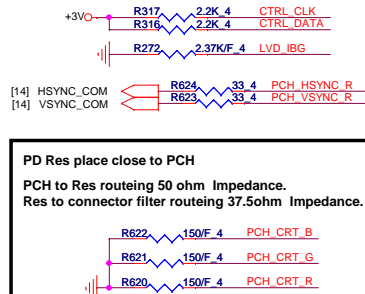
Cougar Point (LVDS,DDI)



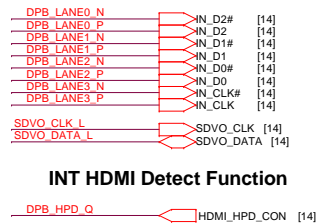
PCH Pull-high/low(CLG)



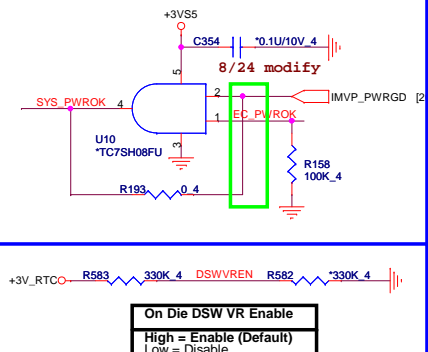
**INT LVDS & CRT disable
(DIS only remove)**



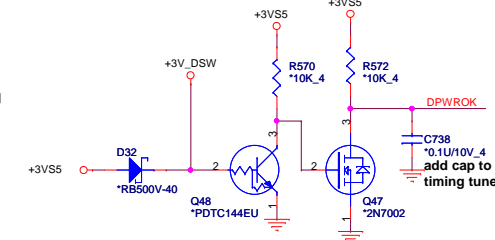
INT HDMI disable (DIS only remove)



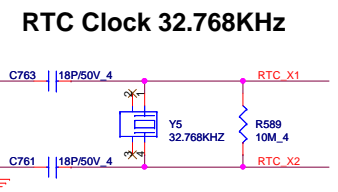
System PWR_OK(CLG)



DPWROK FOR DSW



07



ODD (SATA3 6.0Gb/s)

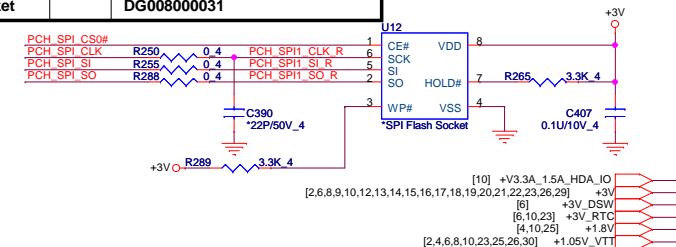
[illegible]

Figure 10 shows the ACZ pin connections for the NDA Base (CEU). The connections are as follows:


- ACZ_BCLK:** Connected to BIT_CLK_AUDIO (R273) and BIT_CLK_MDC (R276).
- ACZ_RST#:** Connected to ACZ_RST#_AUDIO (R274) and ACZ_RST#_MDC (R275).
- ACZ_SDOUT:** Connected to ACZ_SDOUT_AUDIO (R601) and ACZ_SDOUT_MDC (R604).
- ACZ_SYNC_AUDIO:** Connected to ACZ_SYNC_AUDIO (R613) and ACZ_SYNC_MDC (R612).
- ACZ_SYNC_MDC:** Connected to ACZ_SYNC_MDC (R612).

The diagram also shows a 5V0 supply connected to R605 (10K 4) and R657 (1M 4). A 2N7002K MOSFET is connected to the ACZ_SYNC_AUDIO line. A dashed box labeled "For MDC 5/20" encloses the connections for BIT_CLK_MDC, ACZ_RST#_MDC, and ACZ_SDOUT_MDC.

Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031



Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR <i>Different from Calpella</i>	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI	0	0	LPC	
GNT1#	GNT0#	Boot Location											
1	1	SPI											
0	0	LPC											
GPIO19 <i>Different from Calpella</i>	Boot BIOS Selection 0 [bit-0]	PWROK											
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)										
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K) [23]										
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
GPIO28 <i>Different from Calpella</i>	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable										

	PROJECT : SWH Quanta Computer Inc.			
	Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)		Rev 1A
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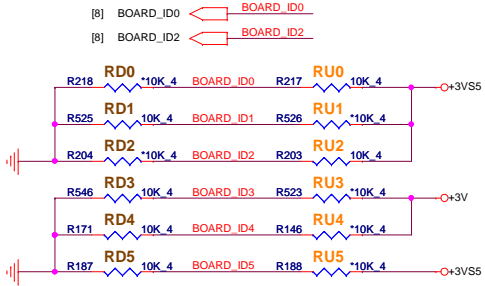
Cougar Point (GPIO,VSS_NCTF,RSVD)



OPTIMUS POWER control pin	
DGPU_PWR0K	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD ID SETTING

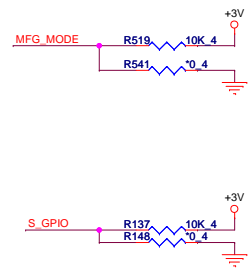
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
15.6" / 14"			0=QLH/TWH 1=QLC/SWH				
dolby				0=NO 1=YES			



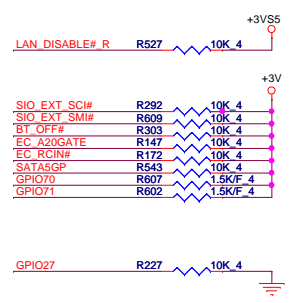
Clock Gen Power OK (CLG)

3/26 DB del external clock generator.

MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

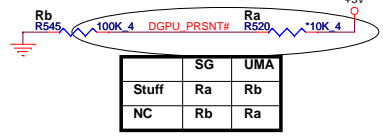
BIOS RECOVERY High = Disable (Default)
Low = Enable

SV_SET_UP
High = Strong (Default)

TEST DETECT
Low = Default

FDI TERMINATION VOLTAGE OVERRIDE LOW - Tx, Rx terminated to same voltage

GFX Present

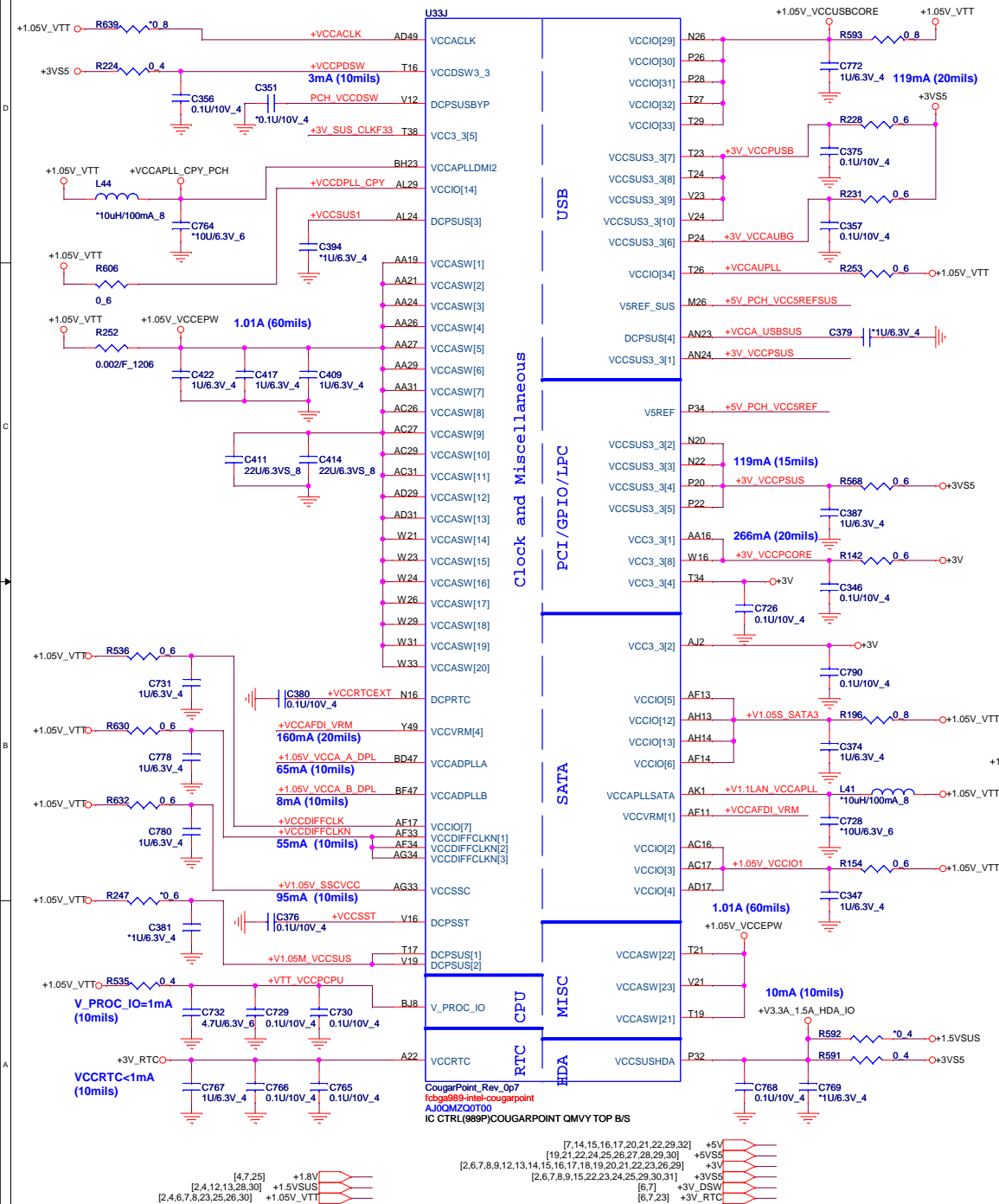


	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

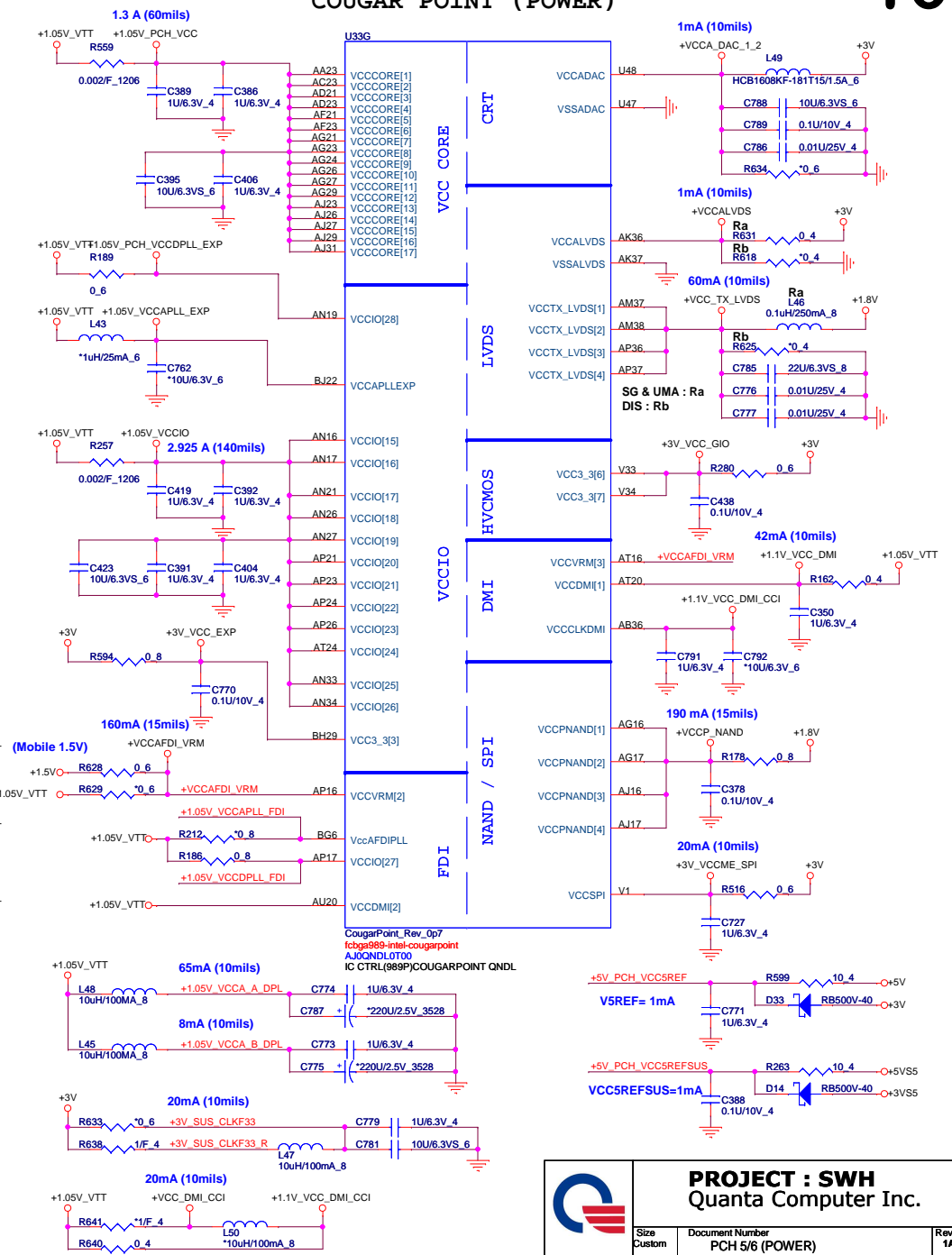
PROJECT : SWH
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
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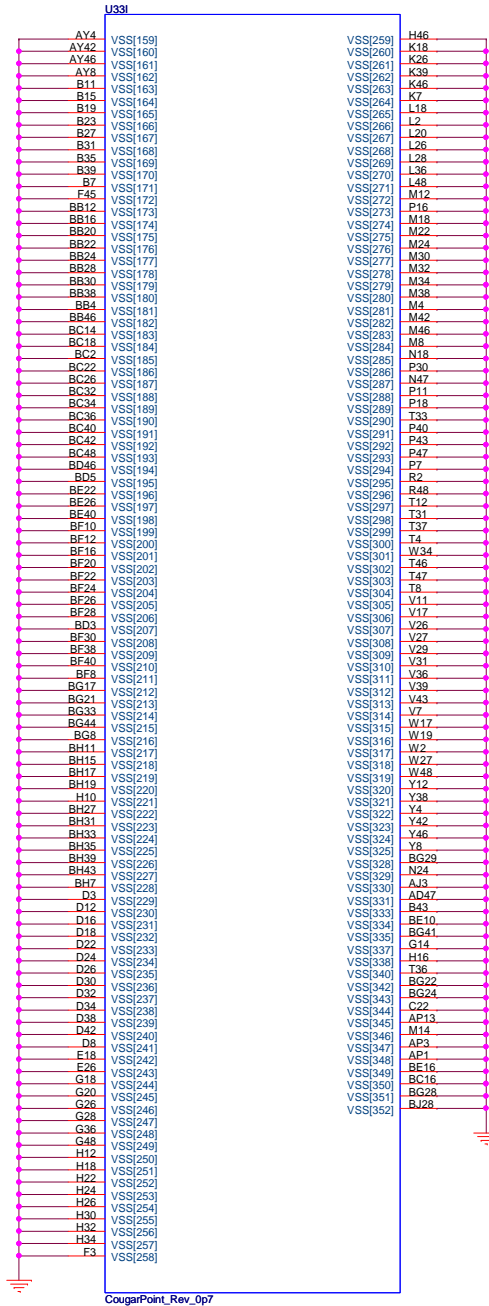
Cougar Point-M (POWER)



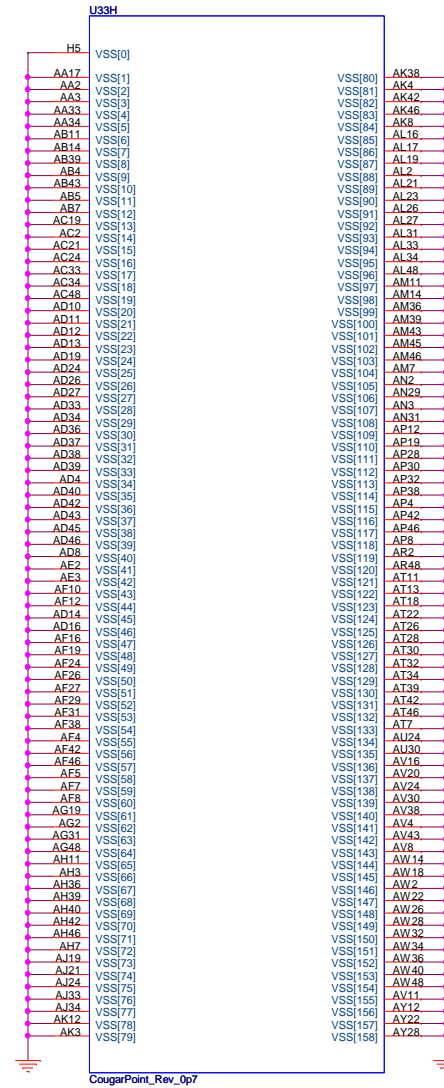
COUGAR POINT (POWER)

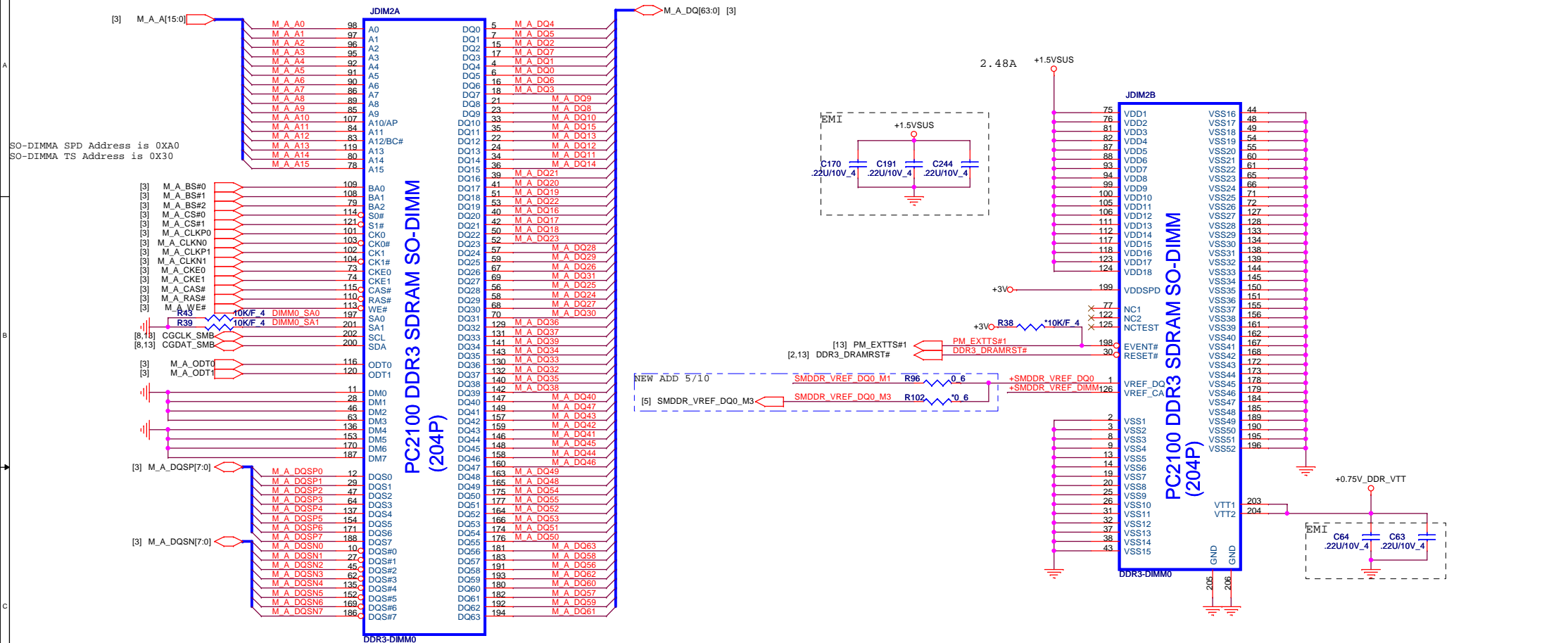


IBEX PEAK-M (GND)



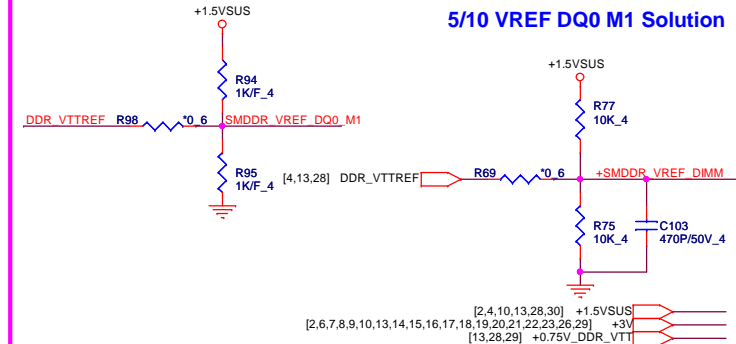
IBEX PEAK-M (GND)



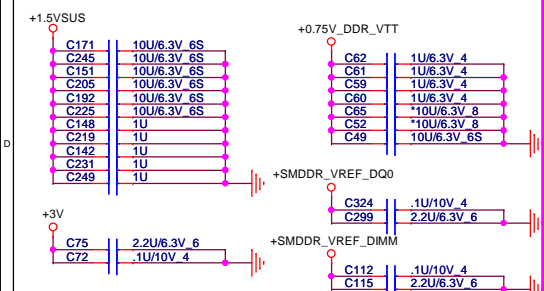


6/22:Document Number: 436996
Intel remove the DDR3 verf M2
circuitry

VREF DQ0 M2 Solution

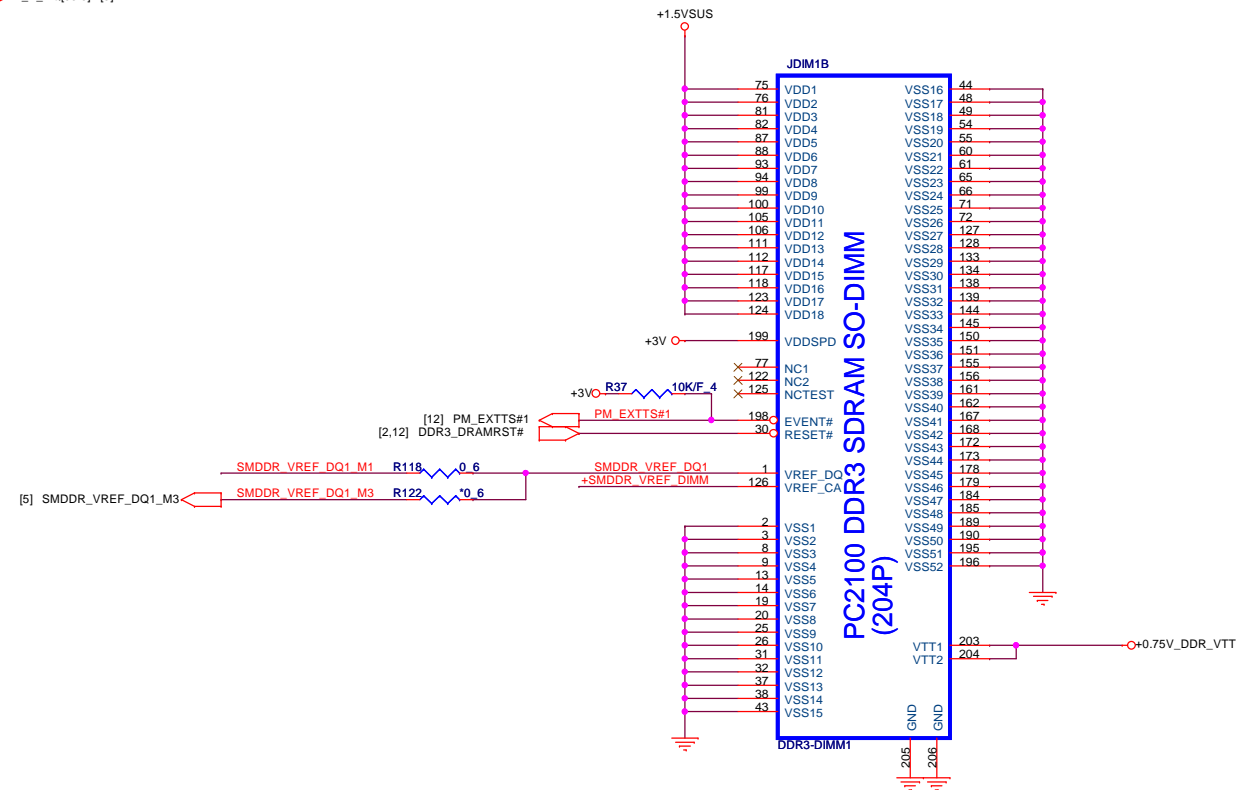
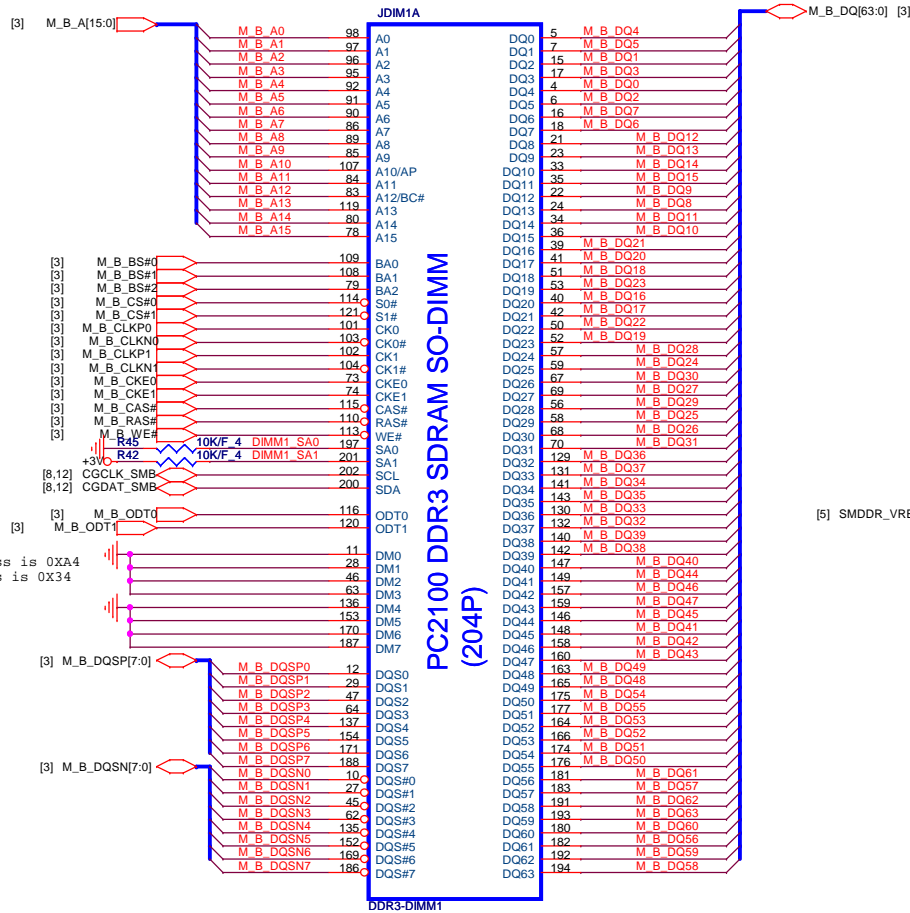


Place these Caps near So-Dimm0.^{11/6}

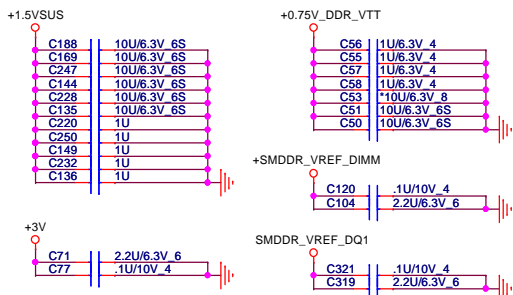


PROJECT : SWH
Quanta Computer Inc.

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Custom	DDR3 DIMM-0	1A
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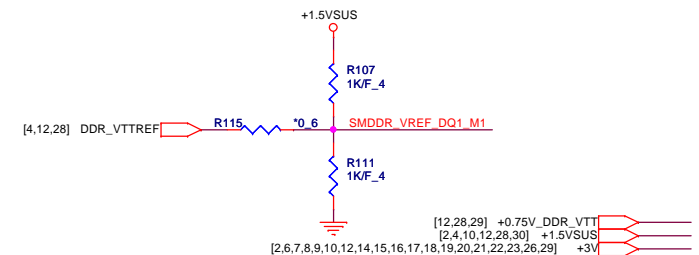
Place these Caps near So-Dimm1.



6/22:Document Number: 436996
Intel remove the DDR3 verf M2
circuitry

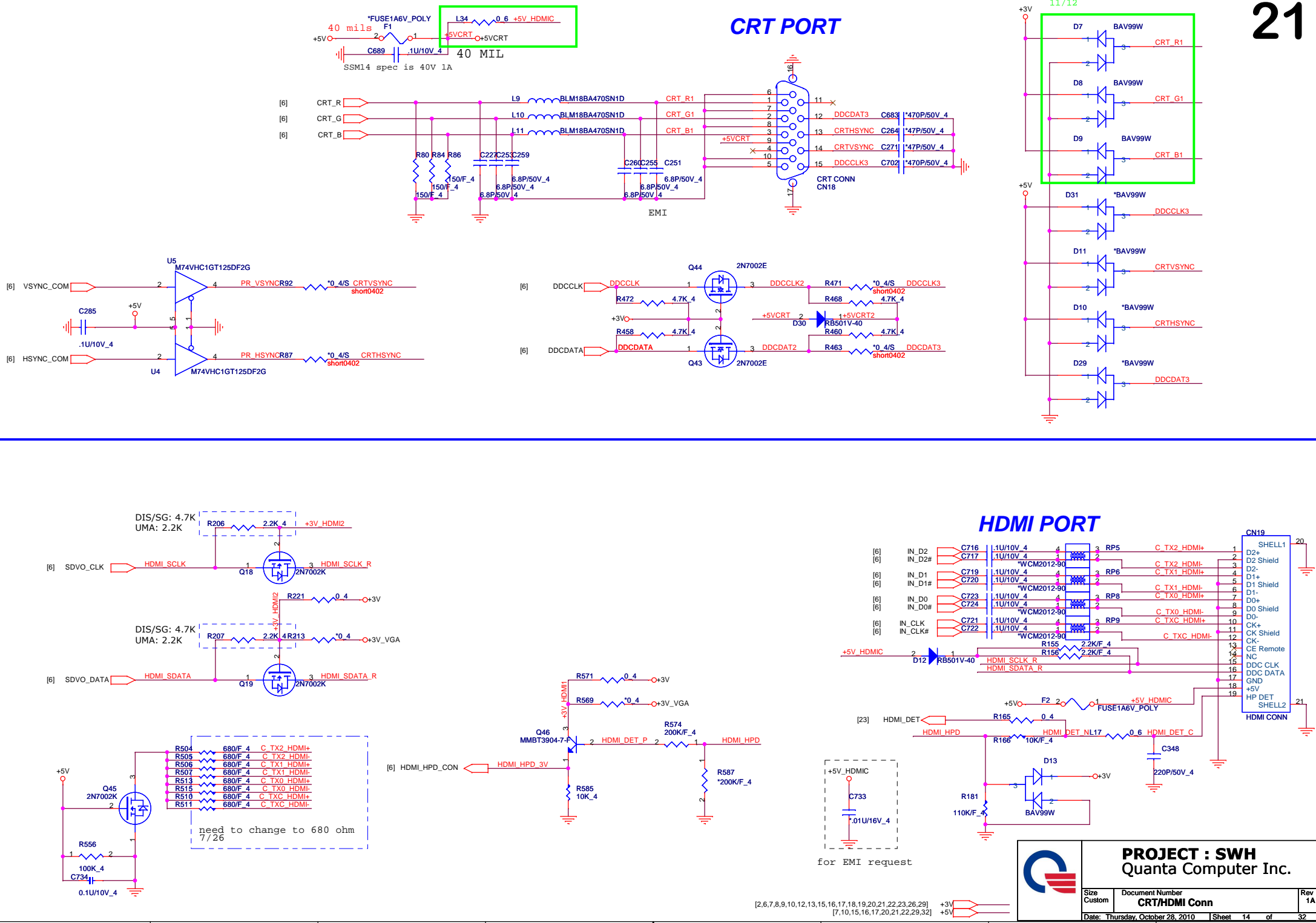
VREF DQ1 M2 Solution

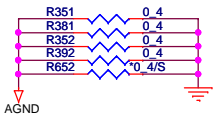
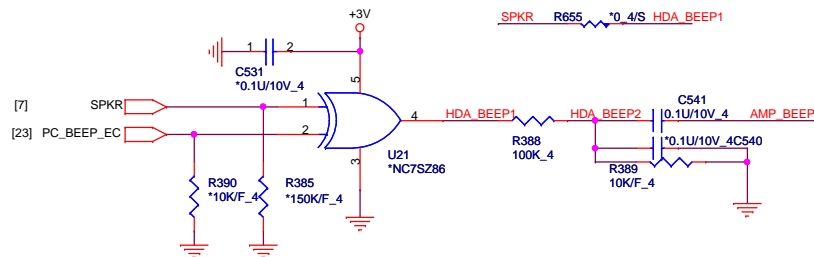
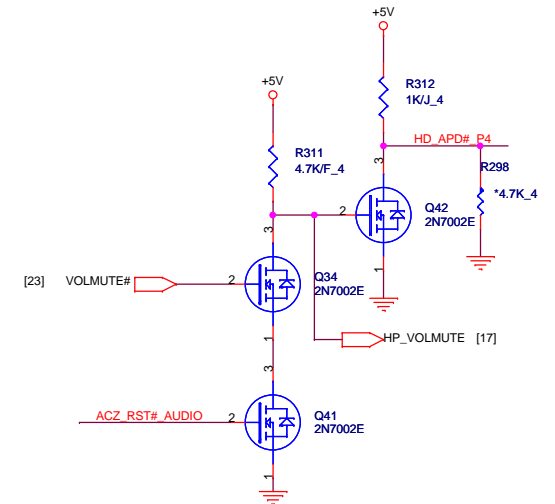
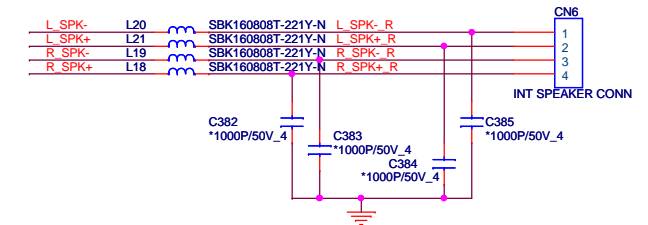
VREF DQ1 M1 Solution

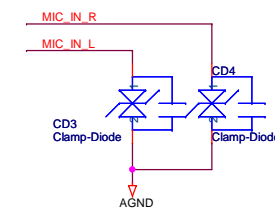
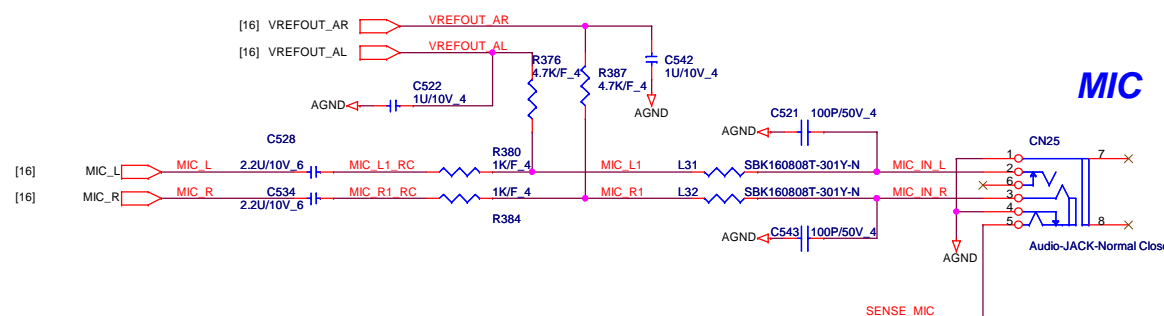
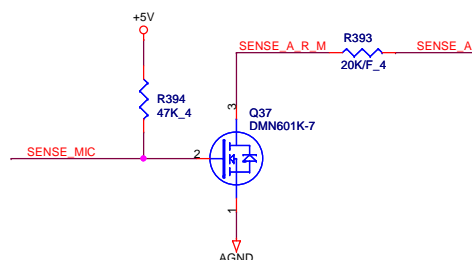
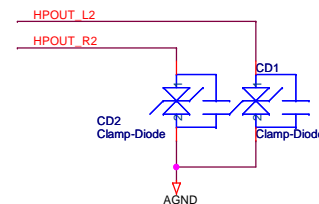
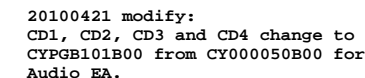


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Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A
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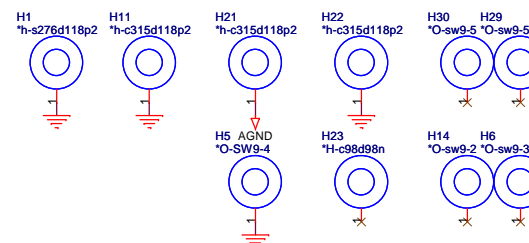
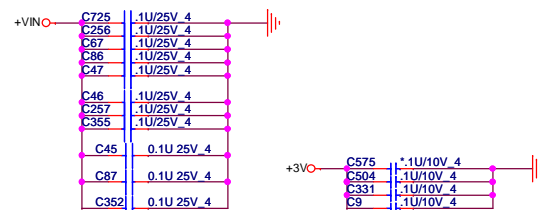
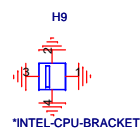




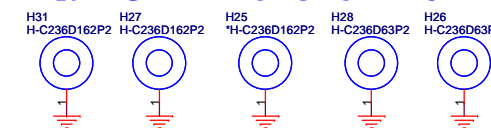
[7,10,14,15,16,20,21,22,29,32] +5V

[2,6,7,8,9,10,12,13,14,15,16,18,19,20,21,22,23,26,29] +3V

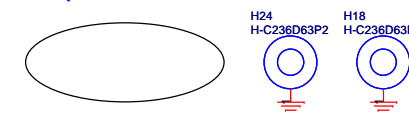
PAD and HOLE



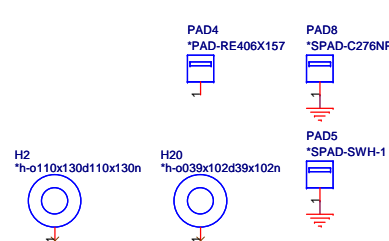
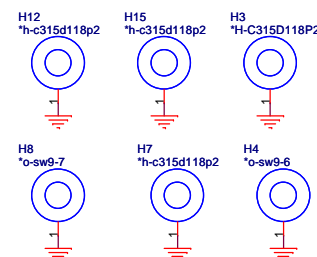
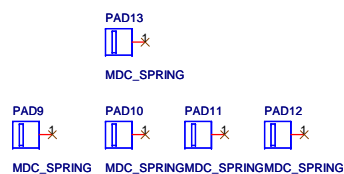
MINI CARD Hole on BOT Side

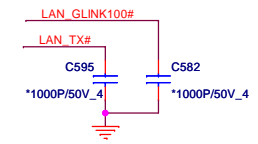


MDC/SB Hole on TOP Side



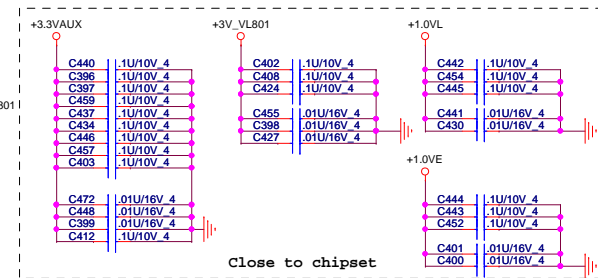
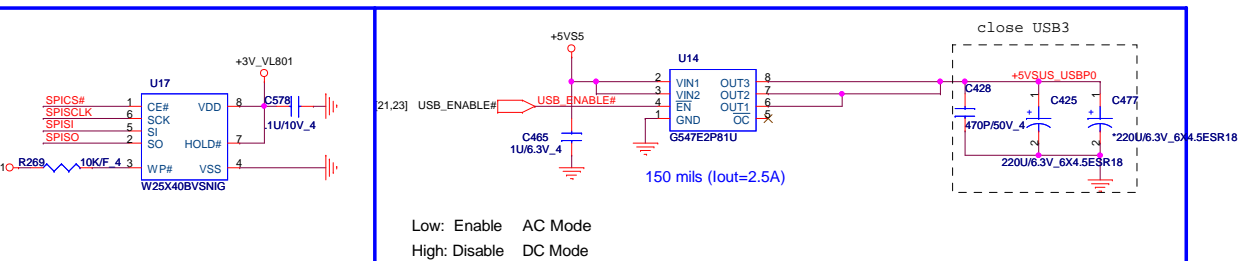
Modem SPRING



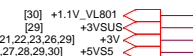
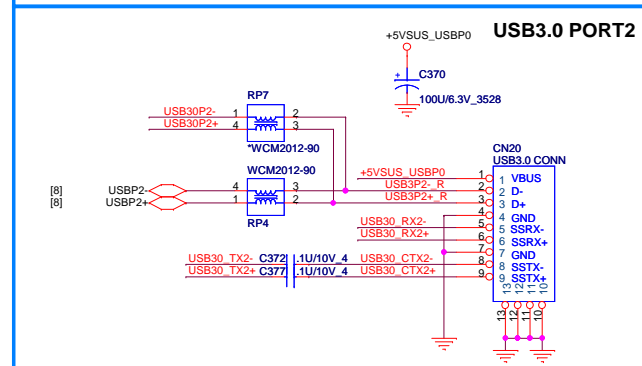


The schematic diagram illustrates the LAN interface circuit. It features two RS501V-40 transceivers, labeled D5 and D4. Transceiver D5 is connected to LAN_GLINK100# and LAN_GLINK100#/1000#. Transceiver D4 is connected to LAN_GLINK100# and LAN_GLINK100#/1000#. The circuit also includes a 0.01uF/16V capacitor (C15) and a 0.4 ohm resistor (R5) connected to LAN_AGN and LAN_AGNND.

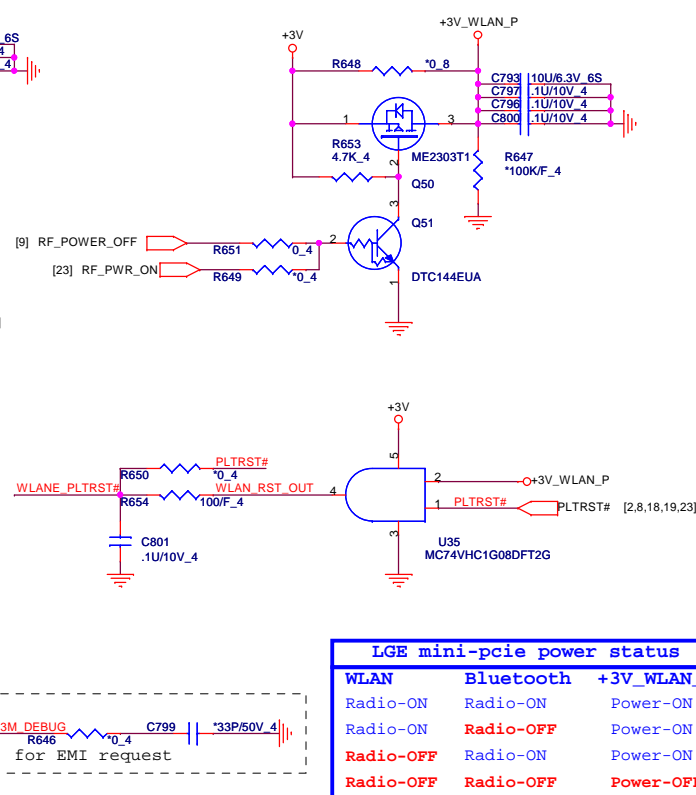
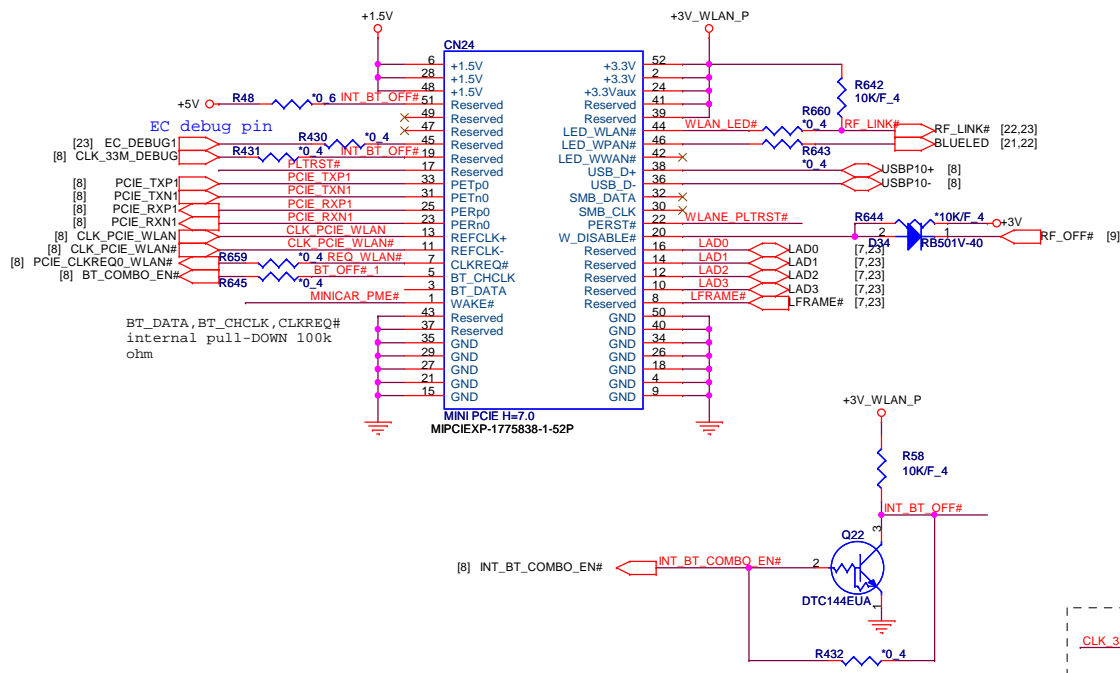
[2,6,7,8,9,10,12,13,14,15,16,17,19,20,21,22,23,26,29] +3V
[29] +3VLAVCC



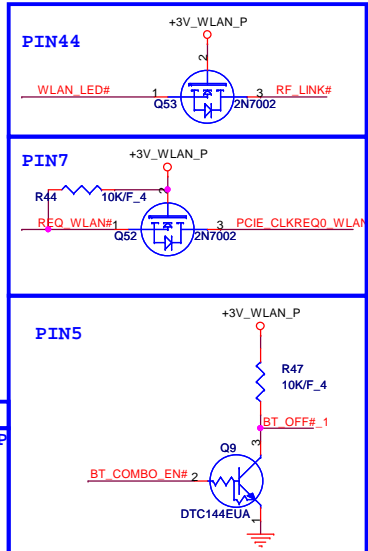
USB3.0/USB2.0 COMBO



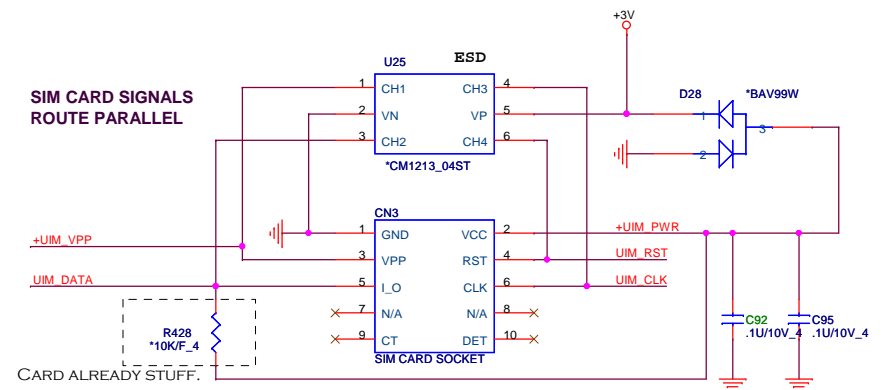
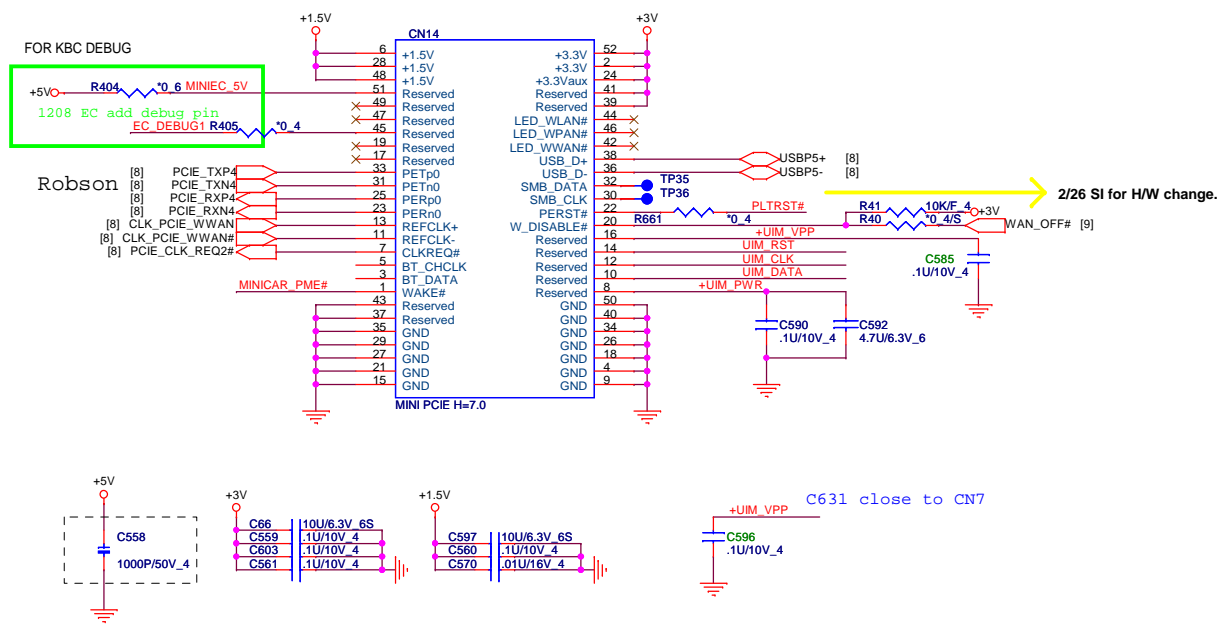
Mini PCI-E Card 1 WLAN



Avoid leakage issue



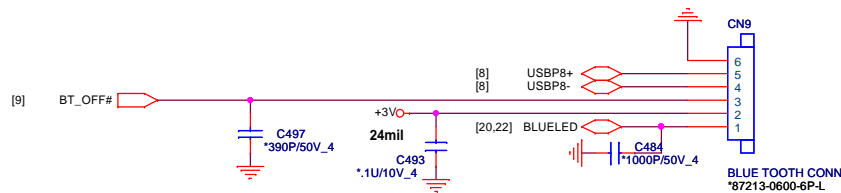
Mini PCI-E Card 2



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Quanta Computer Inc.

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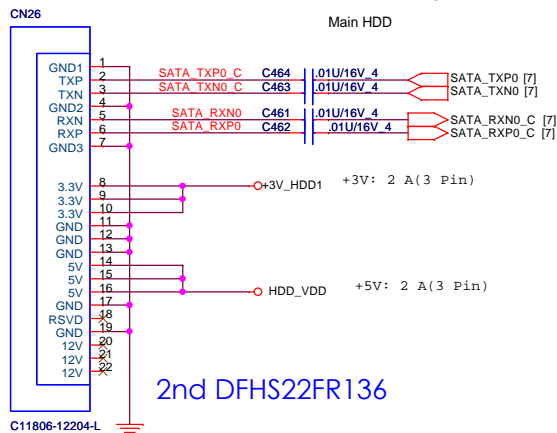
Bluetooth



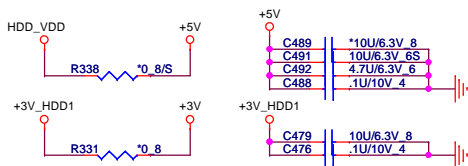
SATA_1 CONNECTOR

DC Current rating: 0.5 A

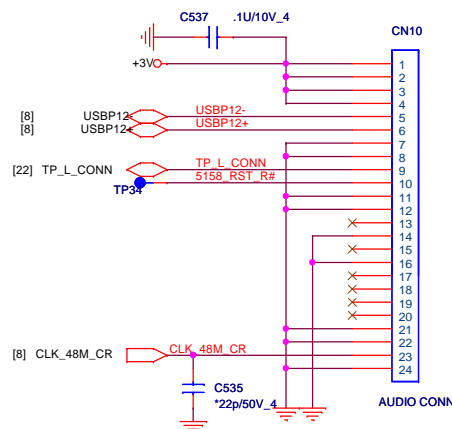
Main HDD



2nd DFHS22FR136

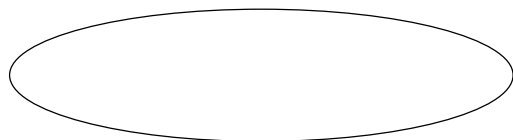


M/B to Cardreader small board

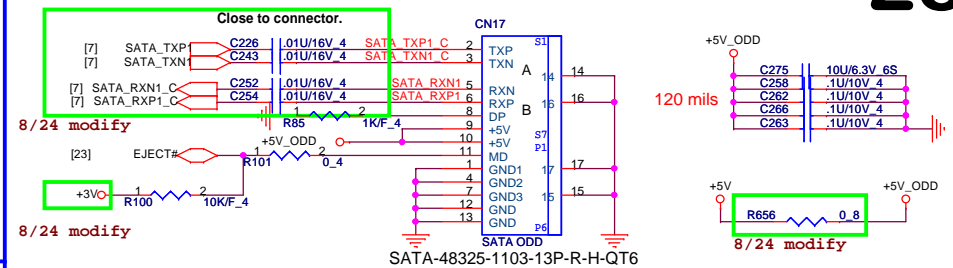


PV Change CN2 footprint 88501-2001-24p-I-nb5

MDC CONNECTOR



SATA ODD

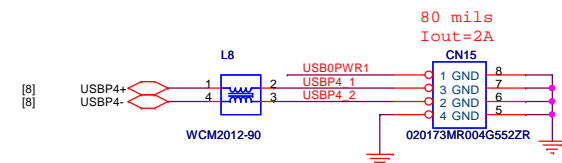
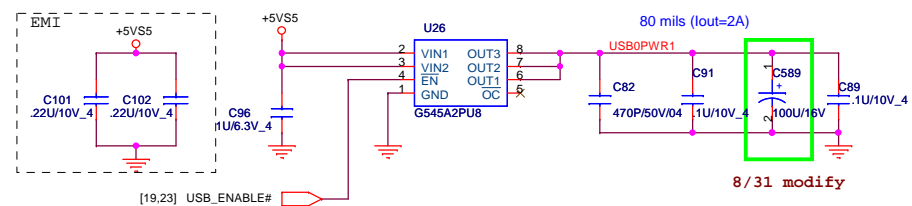


High : ODD power down
Low : ODD power on


ODD_PD R126 *0.4

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USB CONNECTOR

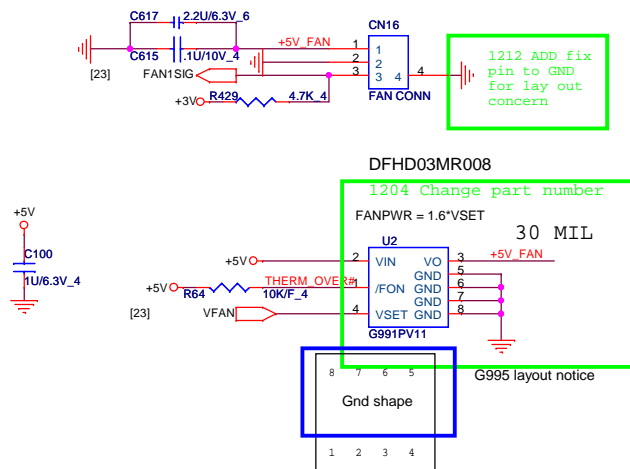


PQ Add ESD Protector

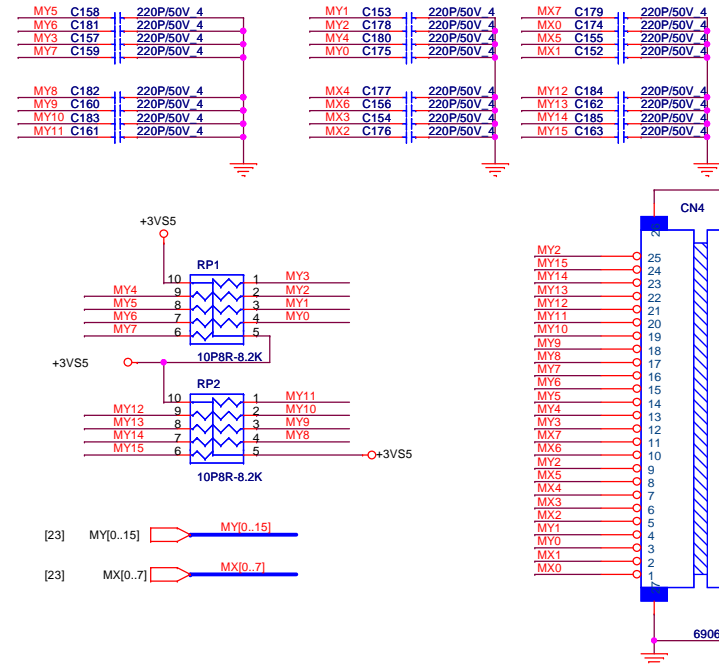
	PROJECT : SWH Quanta Computer Inc.			
	Size Custom	Document Number	Rev 1A	
	ODD/HDD/NEW CARD/TP			
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[2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,22,23,26,29] +3V
[7,10,14,15,16,17,20,22,29,32] +5V
[10,19,22,24,26,27,28,29,30] +5VS5

CPU FAN

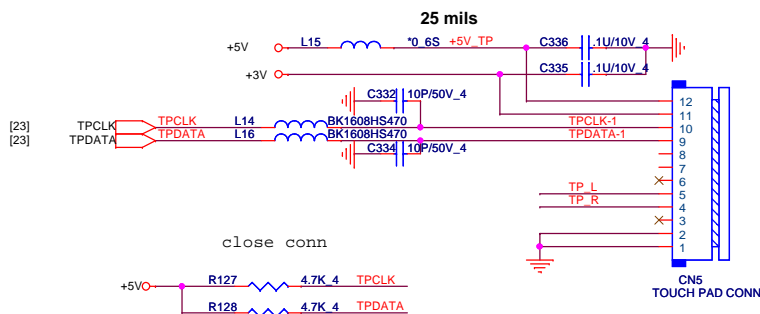


KEYBOARD Con.

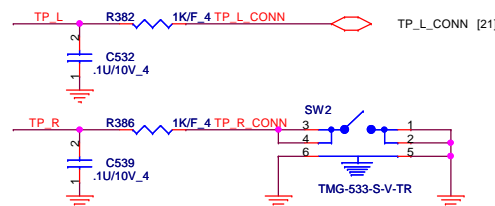


29

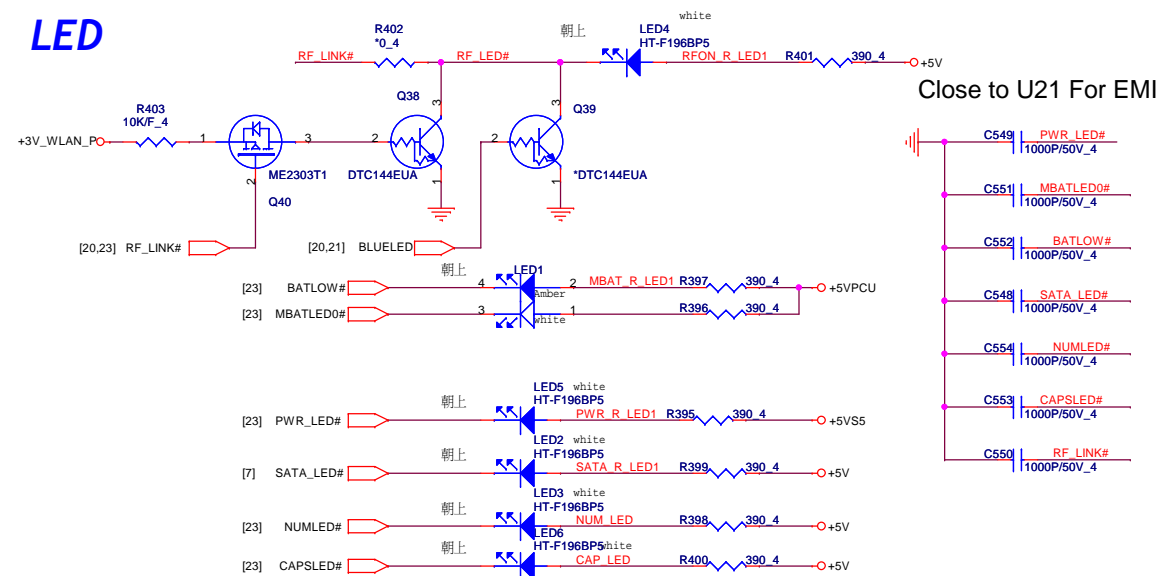
TOUCH PAD CONNECTOR



TOUCH PAD L/R SW1,SW2 in QL2 use, SW3,SW4 in SW9 use



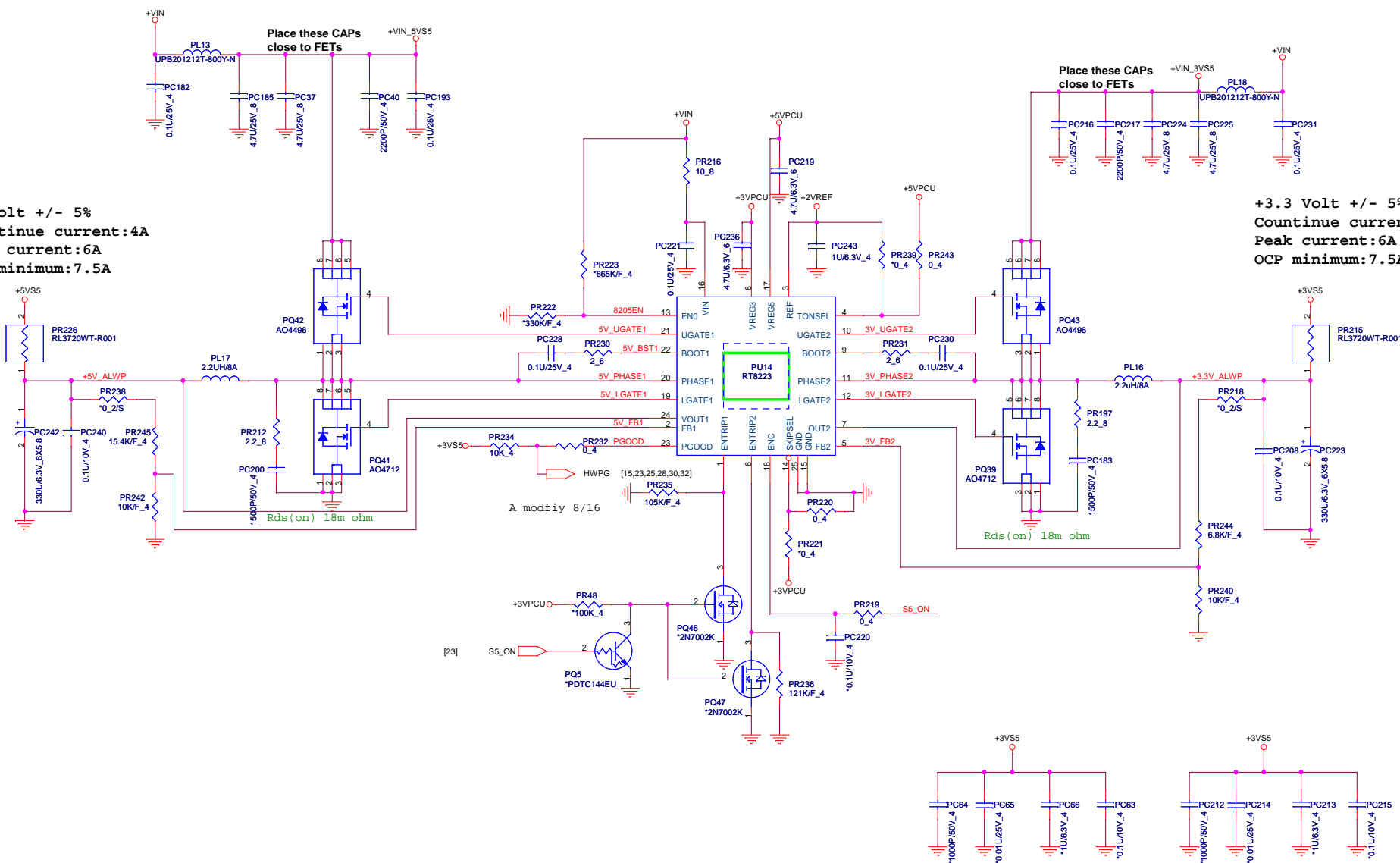
LED

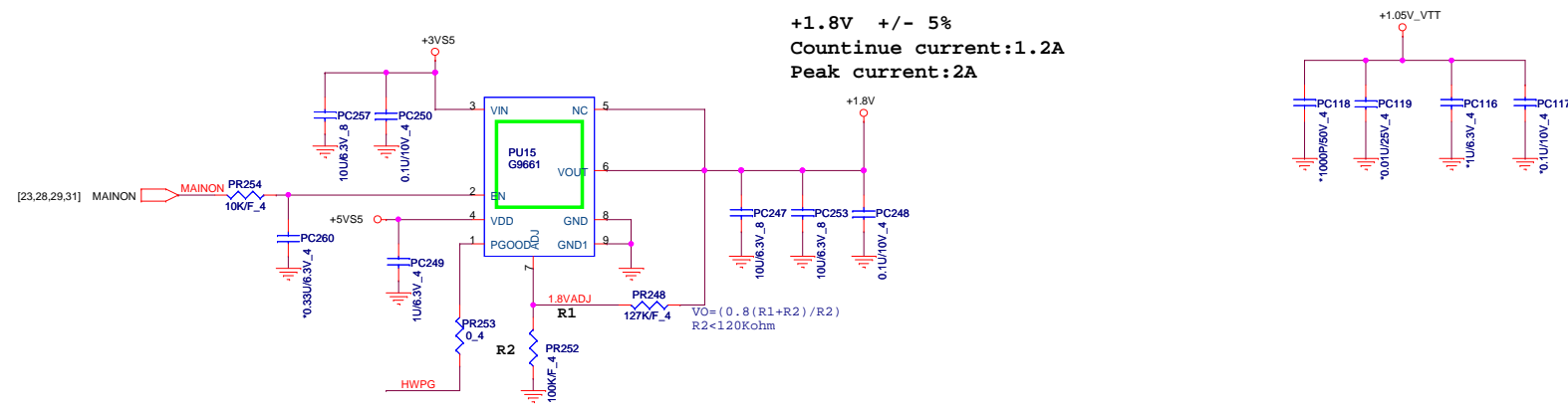
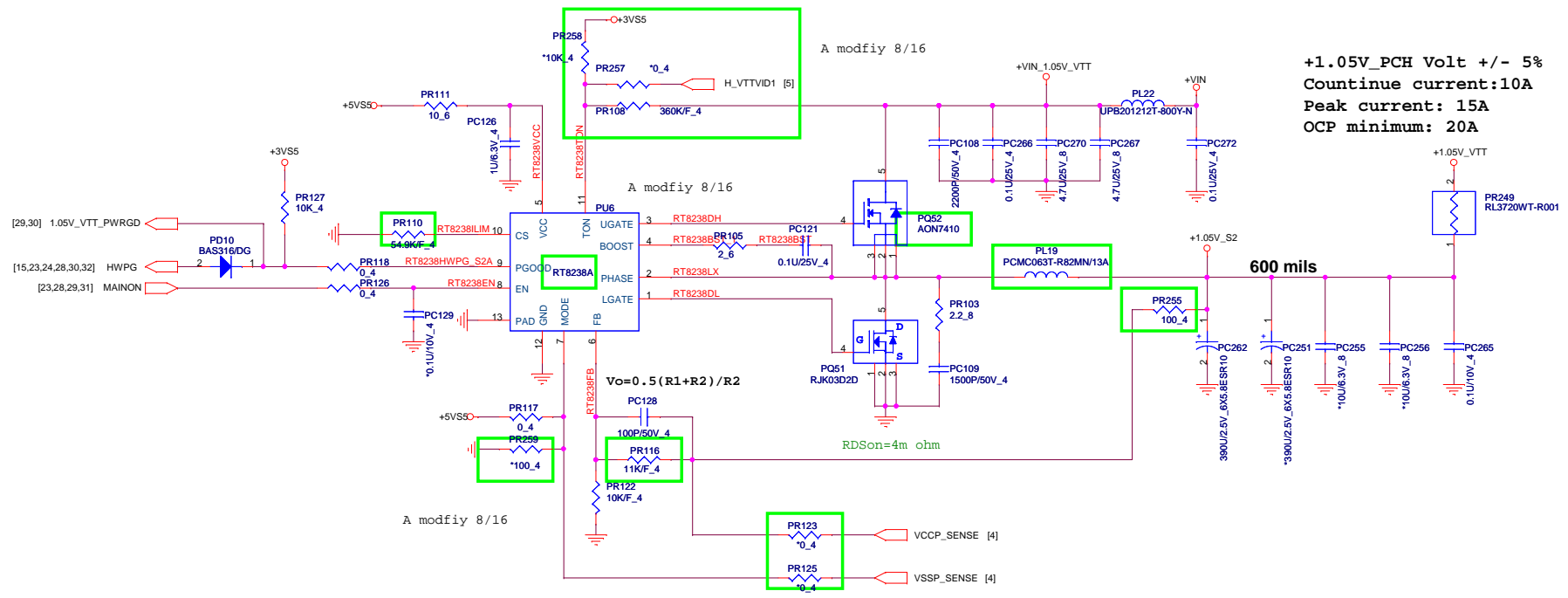


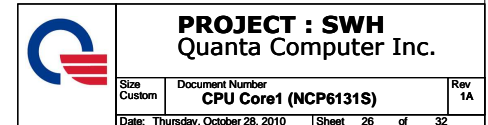
[7,10,14,15,16,17,20,21,29,32]
[2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,21,23,26,29]
[2,6,7,8,9,10,15,23,24,25,29,30,31]

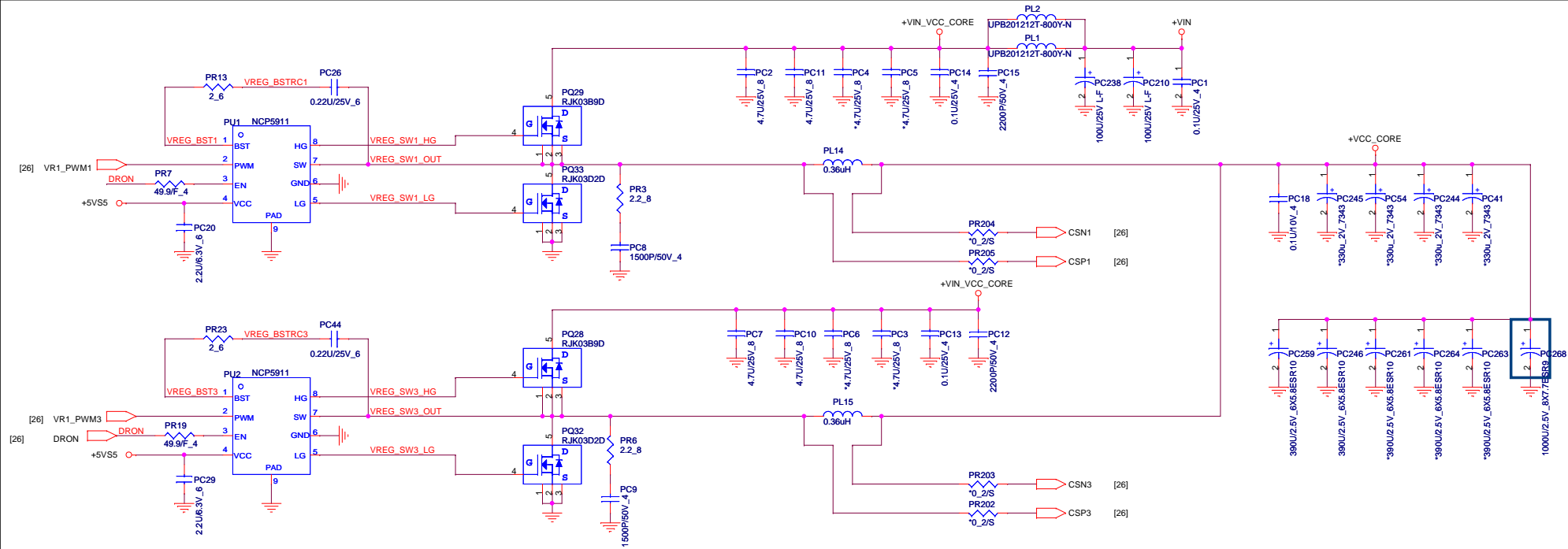
+5 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

+3.3 Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7.5A

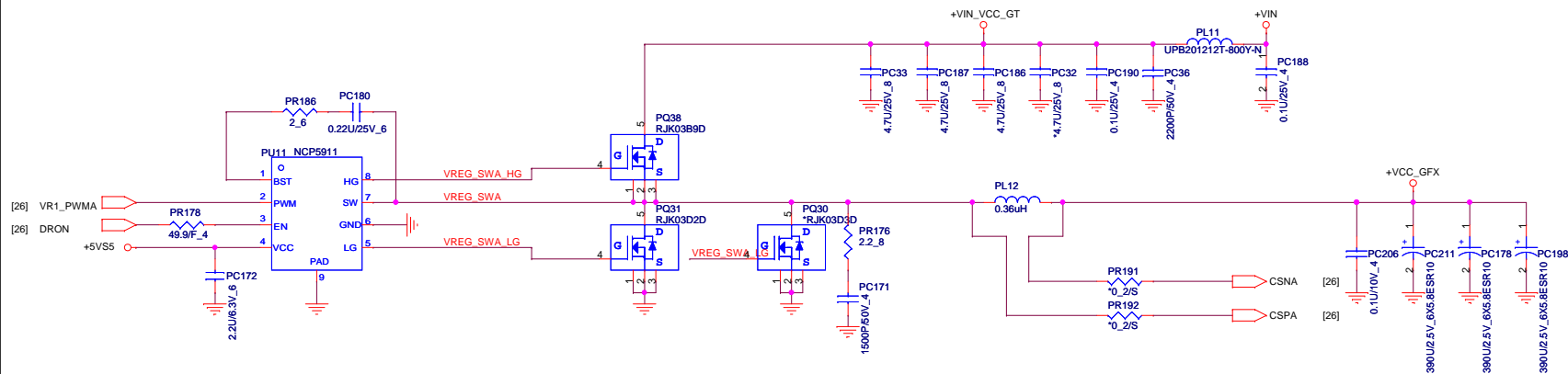






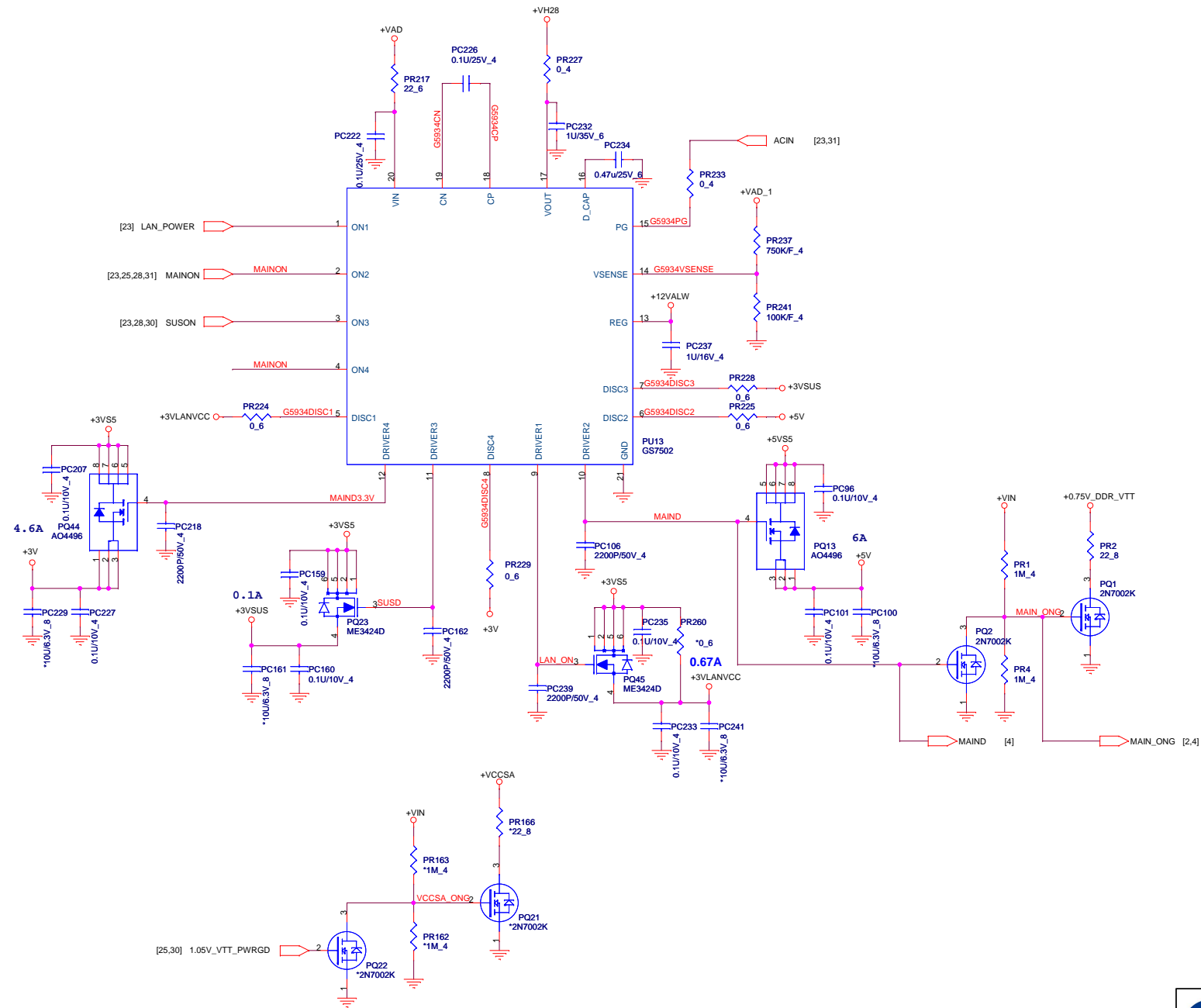


A modfiy 9/16

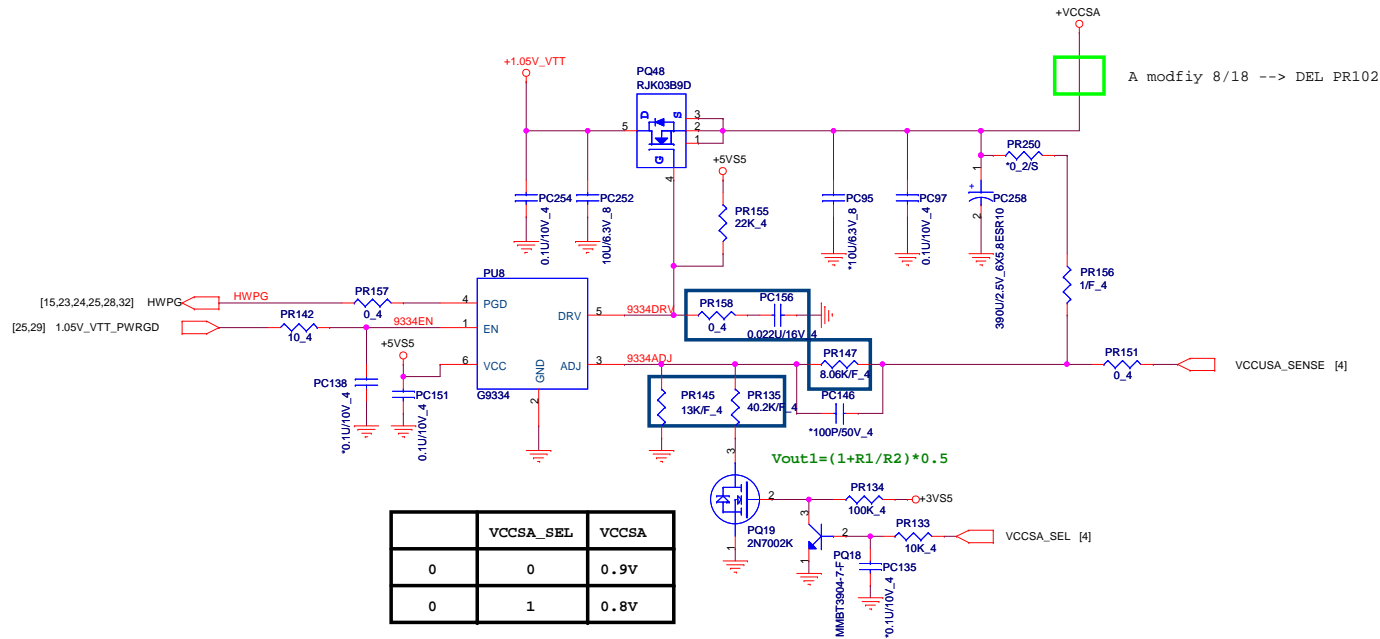


PROJECT : SWH
Quanta Computer Inc.

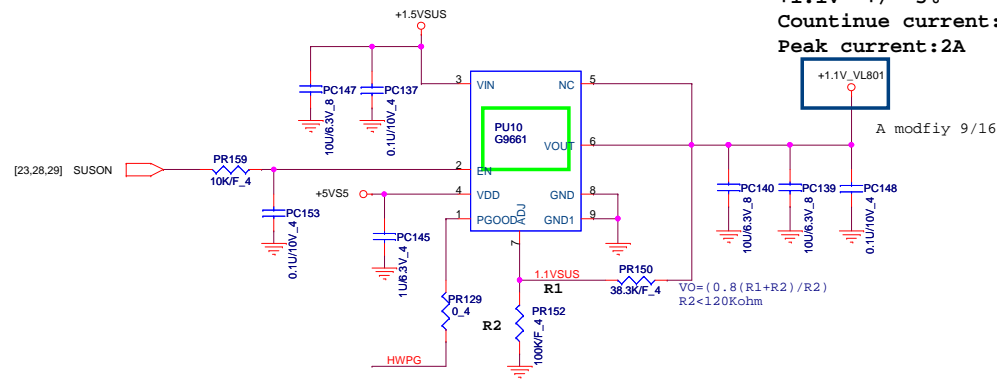
Size	Document Number	Rev
Custom	CPU Core2 (NCP5911)	1A
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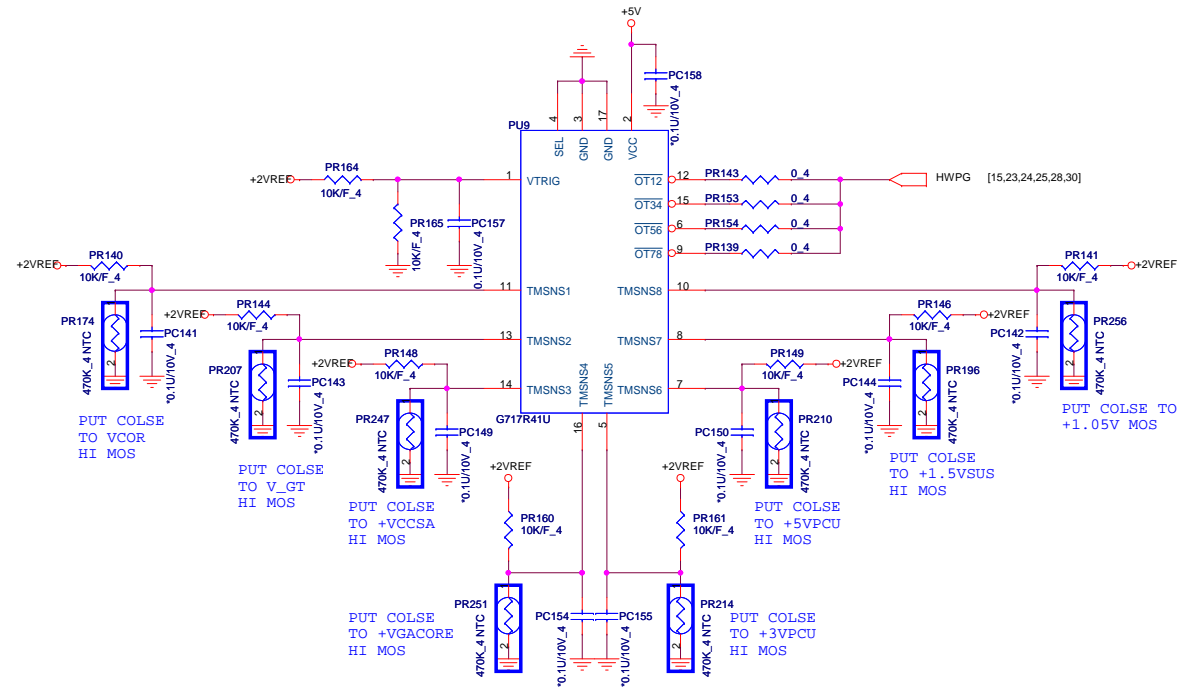
0.85V Volt +/- 5%
Countinue current 3A~6A



+1.1V +/- 5%
Countinue current:1.2A
Peak current:2A







Vender	Size	P/N
EON	128KB 512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB 512KB	AKE35FN0N00 (W25X10BVSNIG) AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

